Ashok B. Mehta

SystemVerilog Assertions and Functional Coverage

Guide to Language, Methodology and Applications

Springer

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Ashok B. Mehta
Los Gatos, CA
USA

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To

My dear wife Ashraf Zahedi

and

My dear parents Rukshmani and Biren Mehta

Foreword

Louis H. Sullivan, an American architect, considered the father of the modern skyscraper, and mentor to Frank Lloyd Wright, coined the phrase "form follows function." The actual quote is "form ever follows function" which is a bit more poetic and assertive than the version that has found its way into the common vernacular. He wrote those words in an article written for Lippincott's Magazine #57 published in March 1896. Here is the passage in that article that contains the famous quote:

> "Whether it be the sweeping eagle in his light or the open apple-blossom, then toiling work horse, the blithe swan, the branching oak, the winding stream at its base, the drifting clouds—over all the coursing sun, form ever follows function, and this is the law. Where function does not change, form does not change. The granite rocks, the ever brooding hills, remain for ages; the lightning lives, comes into shape, and dies, in a twinkling.
>
> It is the pervading law of all things organic and inorganic, of all things physical and metaphysical, of all things human and all things superhuman—of all true manifestations of the head, of the heart, of the soul—that the life is recognizable in its expression, that form ever follows function. This is the law."

Earlier in the article, Sullivan foreshadows his thought with this passage:

> "All things in nature have a shape, that is to say, a form, an outward semblance, that tells us what they are, that distinguishes them from ourselves and from each other."

The precise meaning of this pithy phrase has been debated in art and architecture circles since Sullivan's article was first published. However, it is widely accepted to mean that the form of something—its shape, color, size, etc.—is related to what it does. Water flows, rocks sit, and birds fly.

In his book "The Design of Everyday Things,"(Basic Books 1988) Don Norman discusses a similar concept, the notion of affordances. Norman defines the term as "… the perceived and actual properties of the thing, primarily those fundamental properties that determine just how the thing could possibly be used." He cites some examples: "A chair affords ("is for") support and, therefore, affords sitting. A chair can also be carried. Glass is for seeing through, and for breaking. Wood is normally used for solidity, opacity, support or carving."

Norman's idea turns Sullivan's upside down. He is saying function follows form. The shape, color, size, etc., of an object affects what it does. Nonetheless, both men would likely agree that form and function, whichever drives the other, are inextricably linked.

Software designers have the luxury of choosing the form to fit the function. They are not as constrained by the laws of physics as say, a cabinetmaker. The cabinetmaker must choose materials that will not only look nice, but will withstand the weight of books or dishes or whatever is to be placed on the shelves. Software designers have some constraints with regard to memory space and processing time, but beyond that they have a lot of freedom to build whatever comes to mind.

Sullivan referred to "all things physical and metaphysical." Without much of a stretch we can interpret that to include software, a most abstract human creation. The form of a piece of software is linked to its function. The complex software that verification engineers build, called a testbench, must be designed before it can be built. The verification engineer, like an architect, must determine the form of his creation.

The architecture space is wide open. Computer code, while much more abstract than say, a staircase or a door handle on a car, has a form and a function. The form of computer code is the set of syntactic elements strung together in a program. The function is what the program does when executed, often referred to as its semantics.

A verification engineer is typically presented a set of requirements, often as a design specification, and asked to build a testbench that meets these requirements. Because of the tremendous flexibility afforded by the software medium he must choose the form carefully to ensure that not only meets the requirements, but is easy to use, reusable, and robust. He must choose a form that fits the function.

Often an assertion is just the right thing to capture the essence of some part of a design. The *form* of an assertion is short sequence of text that can be inserted easily without disrupting the design. With their compact syntax and concise semantics assertions can be used to check low-level invariants, protocols, or end-to-end behavior.

The *function* of an assertion, in a simulation context, is to assert that something is always (or never) the case. It ensures that invariants are indeed invariant. Assertions can operate as checkers or as coverpoints. The fact that they can be included in-line in RTL code or in separate checkers, they can be short or long for simple or complex checking makes them invaluable in any testbench.

The wise verification engineer uses all the tools as his disposal to create an effective and easy to use testbench. He will consider the function of the testbench and devise a form that suits the required function. Assertions are an important part of any testbench.

Ashok Mehta has written a book that makes assertions accessible. His approach is very pragmatic, choosing to show you how to build and use assertions rather than engage in a lot of theoretical discussion. Not that theoretical discussion is

irrelevant—it is useful to understand the theoretical underpinnings of any technology. However, there are many other books on that topic. This book fills a gap for practicing engineers where before no text provided the how-tos of building and using assertions in a real-world context.

Ashok opens up the world of assertions to verification engineers who may have thought them too opaque to consider using in a real testbench. He does an especially nice job of deconstructing assertions to show how they work and how to write them. Through detailed examples he shows all the pieces that go into creating assertions of different kinds, and how they fit together. Ashok completes the picture by demonstrating how assertions and coverage fit together.

Part of the book is devoted to functional coverage. He deconstructs the sometimes awkward SystemVerilog syntax of covergroups and coverpoints. Like he has with assertions, he takes the mystery out of building a high-quality coverage model.

With the mysteries of assertions unmasked, you can now include them in your personal vocabulary of testbench forms. This will enable you to create testbenches with more sophisticated function.

February 2013 Mark Glasser

Preface

Having been an end user of EDA tools for over 20 years, I have seen that many new technologies stay on way side, because either the engineers do not have time to learn of new technologies/languages or the available material is too complex to digest. A few years back I decided to tackle this problem by creating a very practical, application-oriented down-to-earth SystemVerilog Assertions (SVA) and Functional Coverage (FC) class for professional engineers. The class was well received and I received a lot of feedback on making the class even more useful. That culminated in over 500 slides of class material just on SVA and FC. Many suggested that I had collected enough material for a book. That is how I ended up on this project with the same goal that the reader should understand the concept clearly in an easy and intuitive manner and be able to apply the concepts to real-life applications right away.

The style of the book is such that the concepts are clarified directly in a slide style diagram with talking points. This will hopefully make it easy to use the book as a quick reference as well. Applications immediately following a topic will further clarify the subject matter and my hope is that once you understand the semantics and applications of a given topic, you are ready to apply that to your daily design work. These applications are modeled such that you should be able to use them in your design with minimal modifications.

This book is meant for both design and verification engineers. As a matter of fact, I have devoted a complete section on the reasons and practicality behind having micro-level assertions written by the design engineers and macro-level assertions written by verification engineers. Gone are the days when designers would write RTL and throw it over the wall for the verification engineer to quality check.

The book covers both IEEE 1800-2005 and IEEE 1800-2009 standard SVA language. Even though I have covered all the features of 1800-2009 standard SVA, please note that over 90 % of these features were not supported by EDA tools as of this writing. In other words, the examples belonging to this language subset are not simulated. I would greatly appreciate feedback on 1800-2009 SVA language examples for any errors or omissions.

Chapter 1 is Introduction to SVA and FC giving a brief history of SVA evolution. It also explains how SVA and FC fall under SystemVerilog umbrella to provide a complete assertions and functional coverage driven methodology.

Part I: System Verilog Assertions (SVA)

Chapter 2 goes in-depth on SVA-based methodology providing detail that you can right away use in your project execution. Questions like "How do I know I have added enough assertions?", "What type of assertions should I add", etc. are explained with clarity.

Chapter 3 describes Immediate Assertions. These are nontemporal assertions allowed in procedural code.

Chapter 4 goes into the fundamentals of Concurrent Assertions to set the stage for the rest of the book. How the concurrent multi-threaded semantics work, when and how assertions get evaluated in a simulation time tick, formal arguments, disabling, etc., are described here.

Chapter 5 describes the so-called sampled value functions such as $rose, $fell, $stable, $past etc.

Chapter 6 is the big one! This chapter describes all the operators offered by the language including Clock Delay with and without range, Consecutive repetition with and without range, nonconsecutive repetition with and without range, 'throughout', 'within', 'and', 'or', 'intersect', 'first_match', 'if..else', etc. Each of the operator description is immediately followed by examples and applications to solidify the concept.

Chapter 7 describes the System Functions and Tasks such as $isunknown, $onehot, etc.

Chapter 8 discusses a very important aspect of the language that being properties with multiple clocks. There is not a single design now a day that uses only a single clock. A simple asynchronous FIFO will have a Read Clock and a Write Clock which are asynchronous. Properties need to be written such that check in one clock domain triggers a check in another clock domain. The chapter goes in plenty detail to demystify semantics to write assertions that cross clock domains. The so-called CDC (Clock Domain Crossing) assertions are explained in this chapter.

Chapter 9 is probably the most useful one describing Local Variables. Without this multi-threaded feature many of the assertions would be impossible to write. There are plenty of examples to help you weed through the semantics.

Chapter 10 is on recursive properties. These are rarely used but are very handy when you want to know that a property holds until another becomes true or false.

Chapters 11–13 describe other useful features such as 'expect', 'assume', and detecting end point of a sequence. The ended and matched end-points of sequences are indeed very practical features.

Chapter 14 is entirely devoted to very powerful and practical features that do not quite fit elsewhere. Of main interest here are the examples/testbench for asynchronous fifo checks, concurrent assertions in procedural code, sequence in Verilog 'always' block sensitivity list, and the phenomenon of a 'vacuous pass'!

Chapter 15 is solely devoted to Asynchronous assertions. The example in this chapter shows why you need to be extremely careful in using such assertions.

Chapter 16 is entirely devoted to 1800-2009 features. There are many useful features added by the language designers. Now if only the EDA vendors would get on board and support them!

Chapter 17 describes six LABs for you to try out. The LABs start with simple example moving gradually onto complex ones.

Note The LABs are available on Springer download site extras.springer.com. All required Verilog files, test benches, and run scripts are included for both PC and Linux OS.

Chapter 18 provides answers to the LABs of Chap. 17.

Part II: System Verilog Functional Coverage (FC)

Chapter 19 provides introduction to Functional Coverage and explains differences with Code Coverage.

Chapter 20 is fully devoted to Functional Coverage including in-depth detail on Covergroups, Coverpoints, and Bins including transition and cross coverage.

Chapter 21 provides practical hints to performance implications of coverage methodology. Do not try to cover everything all the time.

Chapter 22 describes Coverage Options, which you may keep in your back pocket as reference material for a rainy day!

Acknowledgments

I am very grateful to many who helped with review and editing of the book, in particular, Mark Glasser for his excellent foreword and in-depth review of the book, Vijay Akkati for detailed review of the chapters and many good suggestions and Sandeep Goel for motivation as well as editing of the book. I would also like to thank Bob Slee, Tom Slee, Norbert Eng, Joe Chang, and Frank Lee for all things verification.

And last but certainly not the least, I would like to thank my wife Ashraf Zahedi for enthusiasm and encouragement throughout the writing of this book and putting up with long nights and weekends required to finish the book. She is the cornerstone of my life always with a positive attitude to carry the day through up and down of life.

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Chapter 1
Introduction

As is well known in the industry, the design complexity at 28 nm node and below is exploding. Small form factor requirements and conflicting demands of high performance and low power and small area result in ever so complex design architecture. Multi-core, multi-threading and Power, Performance and Area (PPA) demands exacerbate the design complexity and functional verification thereof.

The burden lies on functional and temporal domain verification to make sure that the design adheres to the specification. Not only is RTL (and Virtual Platform level) functional verification important but so is silicon validation. Days when engineering teams would take months to validate the silicon in the lab are over. What can you do during pre-silicon verification to guarantee post-silicon validation is a first pass success.

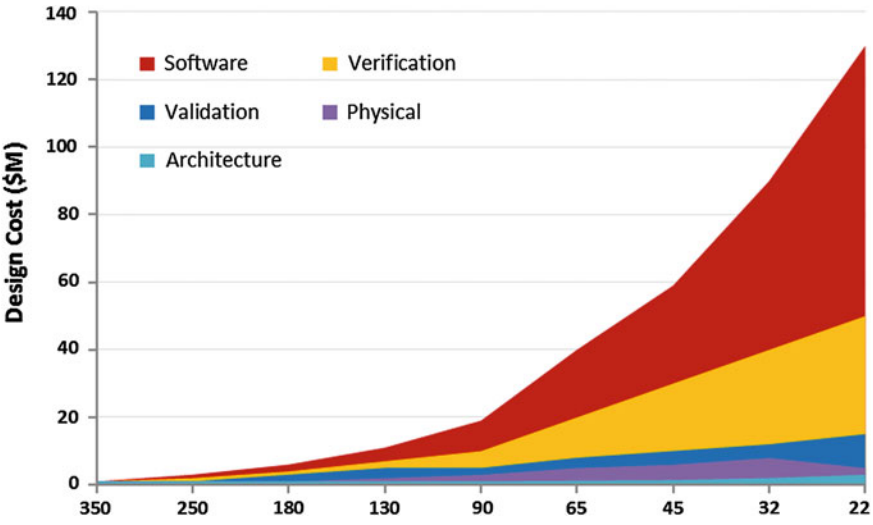

Fig. 1.1 Verification cost increases as the technology node shrinks

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The biggest challenge that the companies face is short time-to-market to deliver first pass working silicon of increasing complexity. Functional design verification is the long poll to design tape-out. Here are two key problem statements.

1. Design Verification Productivity :: 40–50 % of project resources go to functional design verification. The chart in Fig. 1.1 shows design cost for different parts of a design cycle. As is evident, the design verification cost component is about 40+ % of the total design cost. In other words, this problem states that we must increase the productivity of functional design verification and shorten the design ⇔ simulate ⇔ debug ⇔ cover loop. This is a productivity issue, which needs to be addressed (Fig. 1.2).

Continuing with the productivity issue, the following chart shows that the compounded complexity growth rate per year is 58 % while the compounded productivity growth rate is only 21 %. There is a huge gap between what *needs* to get done and what *is* getting done. This is another example of why the productivity of design cycle components such as functional design verification must be improved.

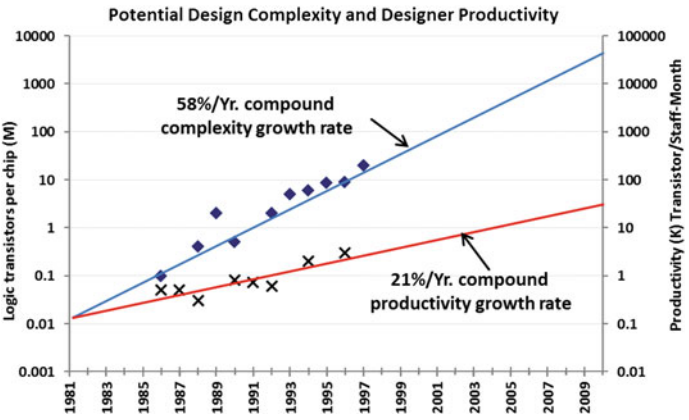


Fig. 1.2 Design productivity and design complexity

2. Design Coverage :: The second problem statement states that more than 50 % of designs require re-spin due to functional bugs. One of the factors that contribute to this is the fact that we did not objectively determine *before* tape-out that we had really *covered* the entire design space with our test-bench. The motto "If it's not verified, it will not work" seems to have taken hold in design cycle. Not knowing if you have indeed covered the entire design space is the real culprit towards escaped bugs and functional silicon failures.

So, what's the solution to each problem statement?

1. Increase Design Verification Productivity

   a. *Reduce Time to Develop*

   i. Raise abstraction level of tests. Use TLM (Transaction Level Modeling) based methodologies such as UVM, SystemVerilog/C++/DPI, etc. The higher the abstraction level, easier it is to model and maintain verification logic. Modification and debug of transaction level logic is much easier, further reducing time to develop test-bench, reference models (scoreboard), peripheral models and other such verification logic.
   ii. Use constrained random verification (CRV) methodologies to reach exhaustive coverage with fewer tests. Fewer tests mean less time to develop and debug.
   iii. Develop Verification Components (UVM agents, for example) that are reusable. Make them parameterized for adoptability in future projects.
   iv. Use SystemVerilog Assertions to reduce time to develop complex temporal domain and combinatorial checks. As we will see, assertions are intuitive and much simpler to model, especially for complex temporal domain checks. Verilog code for a given assertion will be much more lengthy, hard to model and hard to debug. SVA indeed reduces time to develop and debug.

   b. *Reduce Time to Simulate*

   i. Again, higher level of abstraction simulate much faster than pure RTL test bench which is modeled at signal level. Use transaction level test bench.
   ii. Use SystemVerilog Assertions to directly point to the root cause of a bug. This reduces the simulate $\Leftrightarrow$ debug $\Leftrightarrow$ verify loop time. Debugging the design is time consuming as is, but not knowing where the bug is and trial and error simulations further exacerbate the already lengthy simulation time.

   c. *Reduce Time to Debug*

   i. Use SystemVerilog Assertion Based Verification (ABV) methodology to quickly reach to the source of the bug. As we will see, assertions are placed at various places in design to catch bugs where they occur. Traditional way of debug is at IO level. You see the effect of a bug at primary output. You then trace back from primary output until you find the cause of the bug resulting in lengthy debug time. In contrast, an SVA assertion points directly at the source of the failure (for example, a FIFO assertion will point directly to the FIFO condition that failed and right away help with debug of the failure) drastically reducing the debug effort.
   ii. Use Transaction level methodologies to reduce debugging effort (and not get bogged down into signal level granularity)

2. *Reduce Time to Cover* and build confidence in taping out a fully verified design
   i. Use '*cover'* feature of SystemVerilog Assertions to cover complex *temporal* domain specification of your design. As we will see further in the book, 'cover' helps with making sure that you have exercised low level temporal domain conditions with your test-bench. *If an assertion does not fire, that does not necessarily mean that there is no bug*. One of the reasons for an assertion to not fire is that you probably never really stimulated the required condition (antecedent) in the first place. If you do not stimulate a condition, how would you know if there is indeed a bug in the design logic under simulation? 'cover' helps you determine if you have indeed exercised the required temporal domain condition. More on this in later chapters.
   ii. Use SystemVerilog *Functional Coverage* language to measure the '*intent*' of the design. How well have your test bench verified the 'intent' of the design. For example, have you verified all transition of Write/Read/Snoop on the bus? Have you verified that a CPU1-snoop occurs to the same line at the same time that a CPU2-write invalid occurs to the same line? Code Coverage will not help with this. We will cover Functional Coverage in plenty detail in the book.
   iii. Use Code Coverage to cover *structural* coverage (yes, code coverage is still important as the first line of defense even though it simply provides structural coverage). As we will see in detail in the section on SV Functional Coverage, structural coverage does not verify the intent of the design, it simply sees that the code that you have written has been exercised (e.g. if you have verified all 'case' items of a 'case' statement, or toggled all possible assigns, expressions, states, etc.). Nonetheless, code coverage is still important as a starting point to measure coverage of the design.

As you notice from above analysis, SystemVerilog Assertions and Functional Coverage play a key role in about every aspect of Functional Verification. Note that in this book, I use Functional Verification to include both the 'function' functional coverage as well as the 'temporal' functional coverage.

1.1 How Will This Book Help You?

This book will go systematically through each of SystemVerilog Assertions (SVA) and Functional Coverage (FC) language features and methodology components with practical applications at each step. These applications are modeled such that you should be able to use them in your design with minimal modifications. The book is organized using power point style slides and description to make it very easy to grasp the key fundamentals. Advanced applications are given for those users

who are familiar with the basics. For most part, the book concentrates on the in-depth discussion of the features of the languages and shows examples that make the feature easily understandable and applicable. Simulation logs are frequently used to make it easier to understand the underlying concepts of a feature or method.

The book is written by a design engineer for (mainly) hardware design engineers with the intent to make the languages easy to grasp avoiding decipher of lengthy verbose descriptions. The author have been in System and Chip design field for over 20 years and knows the importance of learning new languages and methodologies in shortest possible time to be productive.

The book concentrates on SVA features of the IEEE 1800-2005 standard. Author believes that the features of this standard are plenty to designing practical assertions for the reader's project(s). However, the author have indeed explained IEEE 1800-2009 features in a standalone Chap. 16 to give a flavor of the new standard. Note that many of the 2009 features were not supported by popular simulators as of this writing and the examples provided were not simulated. Please do send your suggestions/corrections to the author.

1.2 SystemVerilog Assertions and Functional Coverage Under IEEE 1800 SystemVerilog Umbrella

SystemVerilog assertions (SVA) and Functional Coverage (FC) are part of IEEE 1800 SystemVerilog standard. In other words, SVA and FC are two of the four distinct language subsets that fall under the SystemVerilog umbrella.

(1) SystemVerilog Object Oriented language for functional verification (using OVM/UVM style libraries)
(2) SystemVerilog language for Design
(3) SystemVerilog Assertions (SVA) language and
(4) SystemVerilog Functional Coverage (FC) Language to see that the verification environment/test-bench have fully verified your design.

As shown in Fig. 1.3, SVA and FC are two of the important language subsets of SystemVerilog.

In any design, there are 3 main components of verification. (1) Stimulus Generators to stimulate the design (2) Response Checkers to see that the device adheres to the device specifications (3) Coverage components to see that we have indeed structurally and functionally covered everything in the DUT according to the device specifications.

(1) *Stimulus Generation*. This entails creating different ways in which a DUT needs to be exercised. For example, a peripheral (e.g. USB) maybe modeled as a Bus Functional Mode (or a UVM (Universal Verification Methodology)

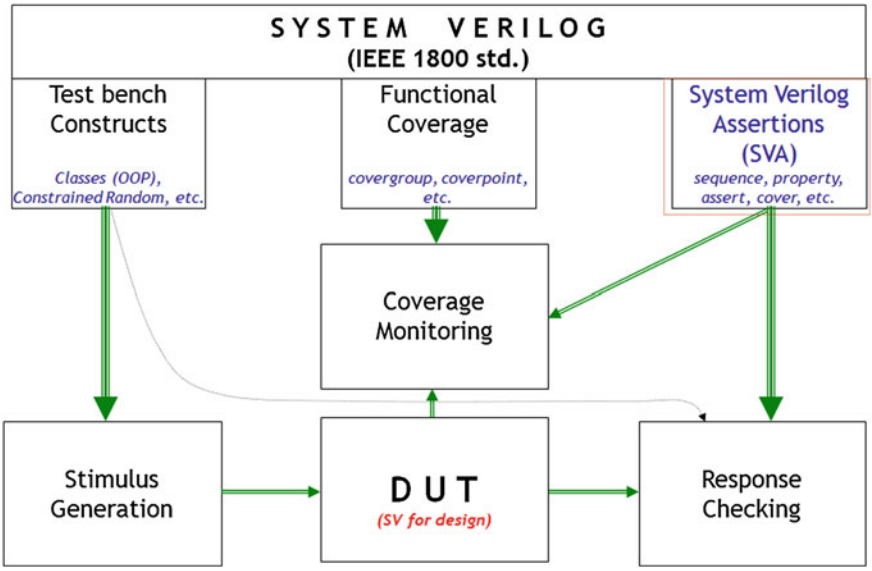


Fig. 1.3 SystemVerilog assertions and functional coverage components under SystemVerilog IEEE 1800-2009 umbrella

agent) to drive traffic through SystemVerilog transactions to the DUT. Different techniques are deployed to achieve exhaustive coverage of the design. For example, constrained random, transaction based, UVM based, memory based, etc. These topics are beyond the scope of this book.

(2) *Response checking*. Now that you have stimulated the DUT, you need to make sure that the device has responded to that stimulus according to the device specs. Here is where SVA comes into picture along with UVM monitors, scoreboards and other such techniques. SVA will check to see that the design not only meets high level specifications but also low level combinatorial and temporal design rules.

(3) *Functional Coverage*. How do we know that we have exercised everything that the device specification dictates? Code Coverage is one measure. But code coverage is only structural. For example, it will point out if a conditional has been exercised. But code coverage has no idea if the conditional itself is correct, which is where Functional Coverage comes into picture (more on this later when we discuss Functional Coverage). Functional coverage gives an objective measure of the design coverage (e.g. have we verified all different cache access transitions (for example, write followed by read from the same address) to L2 from CPU? Code Coverage will not give such measure). We will discuss entire coverage methodology in detail in Chap. 19.

1.3 SystemVerilog Assertions Evolution

To set the stage, here is a brief history of Verilog to SystemVerilog evolution (Figs. 1.4 and 1.5). Starting with Verilog 95, we reached Verilog 2001 with Multi-dimensional arrays and auto variables, among other useful features. Meanwhile, functional verification was eating up ever more resources of a given project. Everyone had disparate functional verification environments and methodologies around Verilog. This was no longer feasible.

Industry recognized the need for a standard language that allowed the design *and* verification of a device and a methodology around which reusable components can be built avoiding multi-language cumbersome environments. Enter Superlog, which was a language with high level constructs required for functional verification. Superlog was donated (along with other language subset donations) to create SystemVerilog 3.0 from which evolved SystemVerilog 3.1, which added new features for design but over 80 % of the new language subset was dedicated to functional verification. We can only thank the Superlog inventor (the same inventor as that for Verilog—namely, Phil Moorby) and the Accelera technical subcommittees for having a long term vision to design such a robust all-encompassing language. No multi-language solutions were required any more. No more reinventing of the wheel with each project was required anymore.

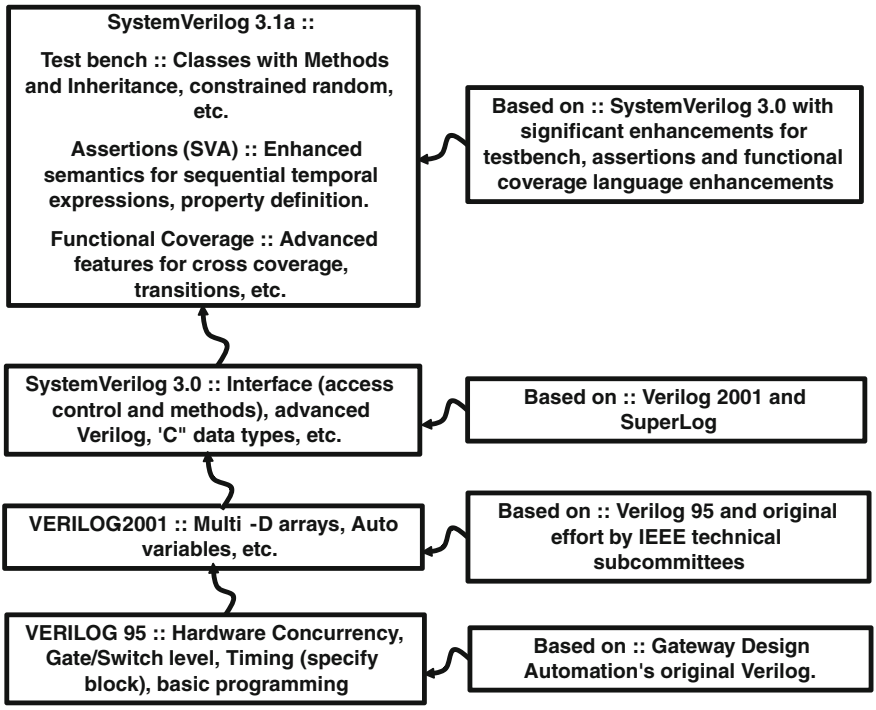


Fig. 1.4 SystemVerilog evolution

As shown in Fig. 1.5, SystemVerilog Assertion language is derived from many different languages. Features from these languages either influenced the language or were directly used as part of the language syntax/semantic.

Sugar from IBM led to PSL. Both contributed to SVA. The other languages that contributed are Vera, 'e', CBV from Motorola and ForSpec from Intel.

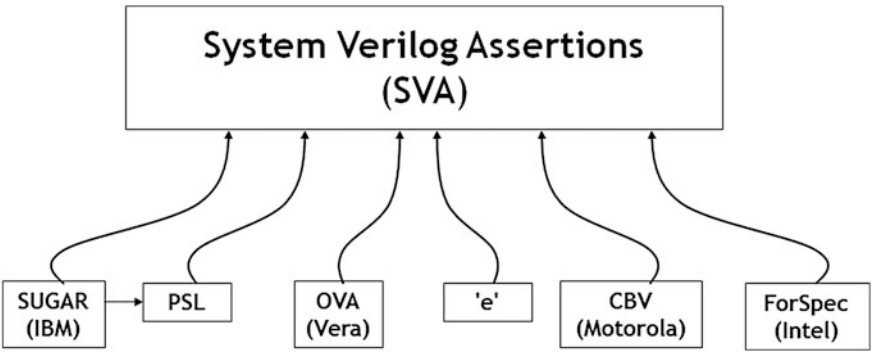


Fig. 1.5 SystemVerilog assertion evolution

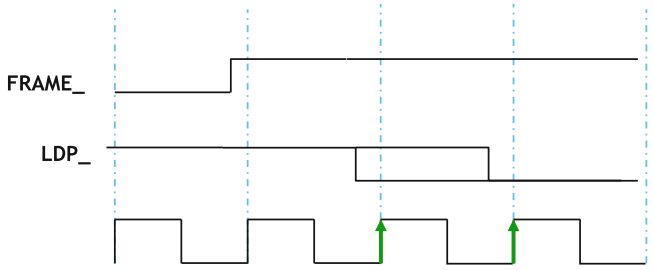
In short, when we use SystemVerilog Assertions language, we have the benefit of using the latest evolution of an assertions language that benefited from many other robust assertions languages.

Chapter 2
System Verilog Assertions

2.1 What is an Assertion?

An assertion is simply a check against the specification of your design that you want to make sure never violates. If the specs are violated, you want to see a failure.

A simple example is given below. Whenever FRAME_ is de-asserted (i.e. goes High), that the Last Data Phase (LDP_) must be asserted (i.e. goes Low). Such a check is imperative to correct functioning of the given interface. SVA language is precisely designed to tackle such temporal domain scenarios. As we will see in Sect. 2.2.1, modeling such a check is far easier in SVA than in Verilog. Note also



When FRAME_ is de-asserted, LDP_ (last data phase) must be asserted within the next 2 clocks

```
property ldpcheck;
  @(posedge clk) $rose (FRAME_) |-> ##[1:2] $fell (LDP_);
endproperty

aP: assert property (ldpcheck) else $display("ldpcheck FAIL");
cP: cover property (ldpcheck) $display("ldpcheck PASS");
```

Fig. 2.1 A simple bus protocol design and its SVA property

A. B. Mehta, *SystemVerilog Assertions and Functional Coverage*,
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that assertions work in temporal domain (and we will cover a lot more on this later); and are concurrent as well as multi-threaded. These attributes is what makes SVA language so suitable for writing temporal domain checks.

Figure 2.1 shows the assertion for this simple bus protocol. We will discuss how to read this code and how this code compares with Verilog in the immediately following Sect. 2.2.1.

2.2 Why Assertions? What are the Advantages?

As we discussed in the introductory section, we need to increase productivity of the design/debug/simulate/cover loop. Assertions help exactly in these areas. As we will see, they are easier to write than standard Verilog or SystemVerilog (thereby increasing design productivity), easier to debug (thereby increasing debug productivity), provide functional coverage and simulate faster compared to the same assertion written in Verilog or SystemVerilog. Let us see these advantages one by one.

2.2.1 Assertions Shorten Time to Develop

Referring to the timing diagram in Fig. 2.1, let us see how SVA shortens time to develop. The SVA code is very self-explanatory. There is the property 'ldpcheck' that says "at posedge clock, if FRAME_ rises, it implies that within the next 2 clocks LDP_ falls". This is almost like writing the checker in English. We then 'assert' this property, which will check for the required condition to meet at every posedge clk. We also 'cover' this property to see that we have indeed exercised the required condition. But we are getting ahead of ourselves. All this will be explained in detail in coming chapters. For now, simply understand that the SV assertion is easy to write, easy to read and easy to debug.

Now examine the Verilog code for the same check (Fig. 2.2). There are many ways to code this. One of the ways at behavioral level is shown. Here you 'fork' out two procedural blocks; one that monitors LDP and another that waits for 2 clocks. You then disable the entire block ('ldpcheck') when either of the two procedural blocks complete. As you can see that not only is the checker very hard to read/interpret but also very prone to errors. You may end up spending more time debugging your checker than the logic under verification.

Verilog Code

```
always @(posedge FRAME_)
begin : ldpcheck
  @(posedge clk);
  fork
    begin
      @(negedge LDP_) disable ldpcheck;
    end
    begin
      repeat (2) @(posedge clk); $display("ldpcheck FAIL");
      disable ldpcheck;
    end
  join
end
```

Fig. 2.2 Verilog code for the simple bus protocol

2.2.2 Assertions Improve Observability

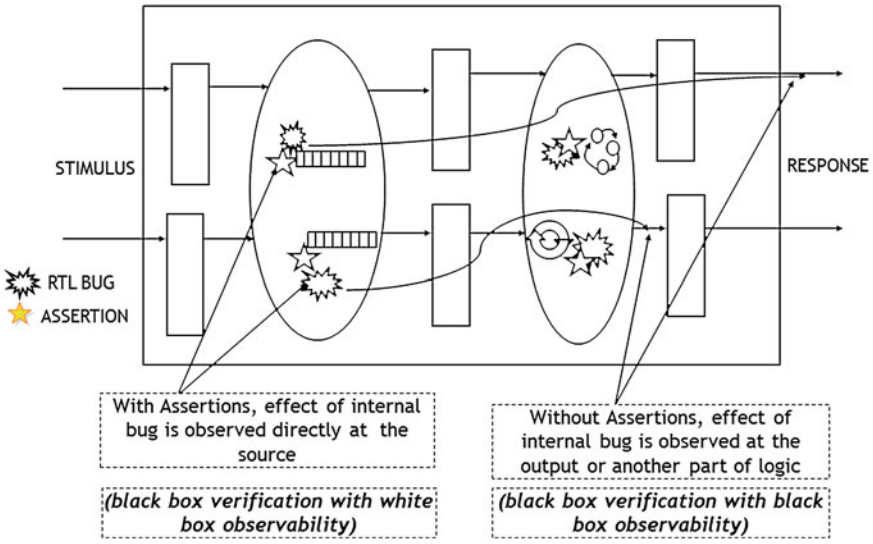


Fig. 2.3 Assertions improve observability

One of the most important advantage of assertions is that they fire at the source of the problem. As we will see in the coming chapters, assertions are located local to temporal conditions in your design. In other words, you don't have to back trace a bug all the way from primary output to somewhere internal to the design where the bug originates. Assertions are written such that they are close to logic (e.g. @

(posedge clk) state0 |-> Read); Such an assertion is sitting close to the state machine and if the assertion fails, we know that when the state machine was in state0 that Read did not take place. Some of the most useful places to place assertions are FIFOs, Counters, block to block interface, block to IO interface, State Machines, etc. These constructs in RTL logic is where many of the bugs originate. Placing an assertion that check for local condition will fire when that local condition fails, thereby directly pointing to the source of the bug (Fig. 2.3).

Traditional verification can be called Black Box verification with Black Box observability, meaning, you apply vectors/transactions at the primary input of the 'block' without caring for what's in the block (blackbox verification) and you observe the behavior of the block only at the primary outputs (blackbox observability). Assertions on the other hand allow you to do black box verification with white box (internal to the block) observability.

2.2.3 Assertions Provide Temporal Domain Functional Coverage

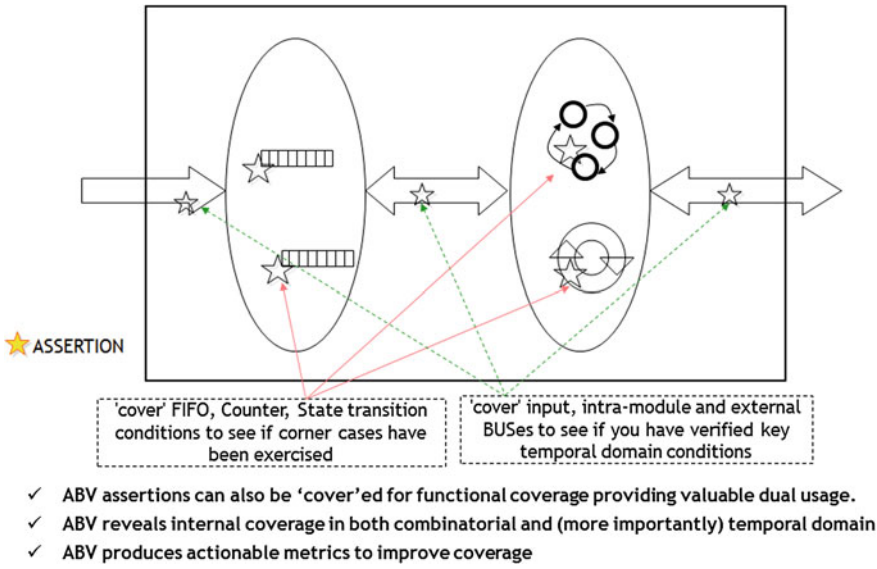


Fig. 2.4 SystemVerilog assertions provide temporal domain functional coverage

Assertions not only help you find bugs but also help you determine if you have covered (i.e. exercised) design logic, mainly temporal domain conditions. They are very useful in finding temporal domain coverage of your test-bench. Here is the reason why this is so important (Fig. 2.4).

Let us say, you have been running regressions 24*7 and have stopped finding bugs in your design. Does that mean you are done with verification? No. Not finding a bug could mean one of two things. (1) There is indeed no bug left in the design or (2) you have not exercised (or covered) all the required functions of the design. You could be continually hitting the same piece of logic in which no further bugs remain. In other words, you could be reaching a wrong conclusion that all the bugs have been found.

In brief, coverage includes three components (we will discuss this in detail in Chap. 19). (1) Code Coverage (which is structural) which needs to be 100 %; (2) Functional Coverage that need to be designed to cover *functionality* of the entire design and must be completely covered; (3) temporal domain coverage (using SVA 'cover' feature) which need to be carefully designed to fully cover all required temporal domain conditions of the design.

Ok, let us go back to the simple bus protocol assertion that we saw in the previous section. Let us see how the 'cover' statement in that SVA assertion works. The code is repeated here for readability.

```
property ldpcheck;
  @(posedge clk) $rose (FRAME_) |-> ##[1:2] $fell (LDP_);
endproperty

aP: assert property (ldpcheck) else $display("ldpcheck FAIL");
cP: cover property (ldpcheck) $display("ldpcheck PASS");
```

In this code, you see that there is a 'cover' statement. What it tells you is "did you exercise this condition" or "did you cover this property". In other words and as discussed above, if the assertion never fires, that could be because of two reasons. (1) you don't have a bug or (2) you never exercised the condition to start with! With the cover statement, if the condition gets exercised but does not fail you get that indication through the 'pass' action block associated with the 'cover' statement. Since we haven't yet discussed the assertions in any detail, you may not completely understand this concept but *determination of temporal domain coverage of your design is an extremely important aspect of verification and must be made part of your verification plan.*

To reiterate, SVA supports the 'cover' construct that tells you if the assertion has been exercised (covered). Without this indication and in the absence of a failure, you have no idea if you indeed exercised the required condition. In our example, if FRAME_ never rises, the assertion won't fire and obviously there won't be any bug reported. So, at the end of simulation if you do not see a bug or you do not even see the "ldpcheck PASS" display, you know that the assertion never fired. In other words, you must see the 'cover property' statement executed in order to know that the condition did get exercised. We will discuss this further in coming chapters. Use 'cover' to full extent as part of your verification methodology.

2.2.3.1 Assertion Based Methodology Allows for Full Random Verification

Huh! What does that mean? This example, I learnt from real life experience. In our projects, we always do full random concurrent verification (i.e. all initiators of the design fire at the same time to all targets of the design) after we are done with directed and constrained random verification. The idea behind this is to find any deadlocks (or livelock for that matter) in the design. Most of the initiator tests are well crafted (i.e. they won't clobber each other's address space) but with such massive randomness, your target model may not be able to predict response to randomly fired transactions. In all such cases, it is best to disable scoreboards in your target models (unless the scoreboards are full proof in that they can survive total randomness of transactions) BUT keep assertions alive. Now, fire concurrent random transactions, the target models will respond the best they can but assertions will pin point to a problem if it exists (such as simulation hang (deadlock) or simply keep clocking without advancing functionality (livelock)).

In other words, assertions are always alive and regardless of transaction stream (random or directed), they will fire as soon as there is the detection of an incorrect condition.

- Example Problem Definition:
  - Your design has Ethernet Receive and Video as Inputs and is also a PCI target.
  - It also has internal initiators outputting transactions to PCI targets, SDRAM, Ethernet Transmit and Video outputs.
  - After you have exhausted constrained random verification, you now want to simulate a final massive random verification, blasting transactions from all input interfaces and firing transactions from internal masters (DMA, Video Engine, Embedded processors) to all the output interfaces of the design.
  - BUT there's a good chance your reference models, self-checking tests, scoreboards may not be able to predict the correct behavior of the design under such massive randomness.
- Solution:
  - Turn off all your checking (reference models, scoreboards, etc.) unless they are full proof to massive random transaction streams.
  - BUT keep Assertions alive.
  - Blast the design with massive randomness (keep address space clean for each initiator).
  - If any of the assertions fire, you have found that corner case bug.

2.2.3.2 Assertions Help Detect Bugs not Easily Observed at Primary Outputs

This is a classic case that we encountered in a design and luckily found before tape-out. Without the help of an assertion, we would not have found the bug and there would have to be a complex software workaround. I will let the following example explain the situation.

- *The Specification*:
  - On a store address Error, the address in Next Address Register (NAR) should be frozen the same cycle that the Error is detected.
- *The Bug*:
  - On a store address error, the state machine that controls the NAR register actually froze the address the next clock (instead of the current address the same clock when store address error occurred). In other words, an incorrect address was being stored in NAR.
- *So, why were the tests passing with this bug*?
  - The tests that were triggering this bug used the same address back to back. In other words, even though the incorrect 'next' address was being captured in NAR, since the 'next' and the 'previous' addresses were the same, the logic would seem to behave correct.
  - *The Assertion*: An assertion was added to check that when a store address error was asserted the state machine should not move to point to the next address in pipeline. Because of the bug, the state machine actually did move to the next stage in pipeline. The assertion fired and the bug was caught.

2.2.3.3 Other Major Benefits

- *SVA language supports Multi- Clock Domain Crossing (CDC) logic*
  - SVA properties can be written that cross from one clock domain to another. Great for data integrity checks while crossing clock domains.
- *Assertions are Readable: Great for documenting and communicating design intent*.
  - Great for creating executable specs.
  - Process of writing assertions to specify design requirements && conducting cross design reviews identify

    Errors, Inconsistencies, omissions, vagueness
  - Use it for design verification (test plan) review.

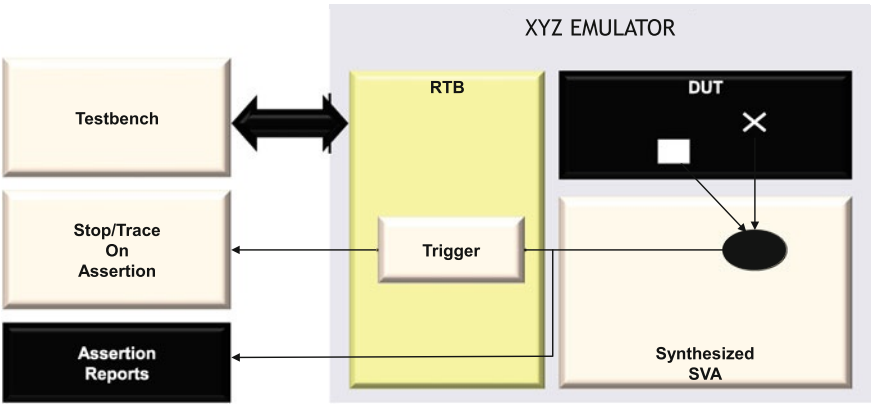
- *Reusability for future designs*
  - Parameterized assertions (e.g. for a 16 bit bus interface) are easier to deploy with the future designs (with a 32 bit bus interface).
  - Assertions can be modeled outside of RTL and easily bound (using 'bind') to RTL keeping design and DV logic separate and easy to maintain.
- *Assertions are always ON*
  - Assertions never go to sleep (until you specifically turn them off).
  - In other words, active assertions take full advantage of every new test/stimulus configuration added by monitoring designs behavior against the new stimulus.
- *Acceleration/Emulation with Assertions*
  - Long latency and massive random tests need acceleration/emulation tools. These tools are beginning to support assertions. Assertions are of great help in quick debug of long/random tests. We will discuss this further in coming sections.
- *Global Severity Levels* ($Error, $Fatal, etc.)
  - Helps maintain a uniform Error reporting structure in simulation.
- *Global turning on/off of assertions* (as in $dumpon/$dumpoff)
  - Easier code management (no need to wrap each assertion with an on/off condition).
- *Formal Verification depends on Assertions*
  - The same 'assert'ions used for design is also used directly by formal verification tools. Static formal applies its algorithms to make sure that the 'assert'ion never fails.
  - 'assume' allows for correct design constraint important to formal.
- *One language, multiple usage*
  - 'assert' for design check and for formal verification
  - 'cover' for temporal domain coverage check
  - 'assume' for design constraint for formal verification.

2.3 How do Assertions Work with an Emulator?

This section is to point out that assertions are not only useful in software based simulation but also hardware based emulation. The reason you can use assertions to fire directly in hardware is because assertions are synthesizable (well, at least the simpler ones). Even though assertion synthesis has ways to go, there is enough of a subset covered by synthesis and that is sufficient to deploy assertions in hardware.

In Fig. 2.5 a generic emulation system is shown. Synthesizable assertions are part of the design that get synthesized and get partitioned to the emulation hardware. During emulation, if the design logic has a bug, the synthesized assertion will fire and trigger a stop/trace register to stop emulation and directly point to the cause of failure.

Anyone who has used emulation as part of their verification strategy, very well know that even though emulator may take seconds to 'simulate' the design, it takes hours thereafter to debug failures. Assertions will be a great boon to the debug effort. Many commercial vendors now support synthesizable assertions.



- **Synthesizable assertions supported by XYZ Emulator**
- **Embedded and bound assertions are automatically synthesized and mapped into the emulator**
- **Assertion reporting and triggering at run-time, similar to simulation**
- **Compile time and Run time control over Assertion compilation and reporting/triggering**

Fig. 2.5 Assertions for hardware emulation

On the same line of thought, assertions can be synthesized in silicon as well. During post-silicon validation, a functional bug can fire and a hardware register can record the failure. This register can be reflected on GPIO of the chip or the register can be scanned out using JTAG boundary scan. The output can be decoded to determine which assertion fired and which part of silicon caused the failure. Without such facility, it takes hours of debug time to pin point the cause of silicon failure. This technique is now being used widely. The 'area' overhead of synthesized assertion logic is negligible compared to the overall area of the chip but the debug facilitation is of immense value. Note that such assertions can make it easier to debug silicon failures in field as well.

2.4 Assertions in Static Formal

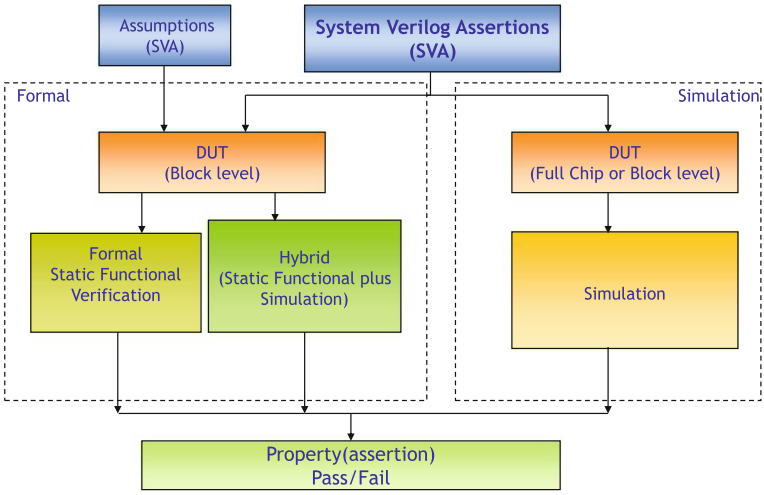


Fig. 2.6 Assertions and assumptions in formal (static functional) and simulation

The same assertions that you write for design verification can be used with static functional verification or the so-called hybrid of static functional plus simulation algorithms. Figure 2.6 shows (on LHS) SVA *Assumptions* and (on RHS/Center) SVA *Assertions*. As you see the assumptions are most useful to *Static Formal Verification (aka Formal)* (even though assumptions can indeed be used in Simulation as well, as we will see in later sections) while SVA assertions are useful in both Formal and Simulation.

So, what is Static Functional Verification (also called Static Formal Functional)? In plain English, static formal is a method whereby the static formal algorithm applies all possible combinational and temporal domain possibilities of inputs to exercise all possible 'logic cones' of a given logic block and see that the assertion(s) are not violated. This eliminates the need for a test-bench and also makes sure that the logic never fails under *any* circumstance. This provides 100 % comprehensiveness to the logic under verification. So as a side note, why do we ever need to write a test-bench!!! The static formal (as of this writing) is limited by the size of the logic block (i.e. gate equivalent RTL) especially if the temporal domain of inputs to exercise is large. The reason for this limitation is that the algorithm has to create different logic cones to try and prove that the property holds. With larger logic blocks, these so-called logic cones explode. This is also known as 'state space explosion'. To counter this problem, simulation experts came up with the *Hybrid Simulation* technique. In this technique, simulation is deployed to 'reach' closer to the assertion logic and then employ the static functional verification algorithms to the logic under assertion checking. This

reduces the scope of the # of logic cones and their size and you may be successful in seeing that the property holds. Since static functional or hybrid is beyond the scope of this book, we'll leave it at that.

2.5 One Time Effort, Many Benefits

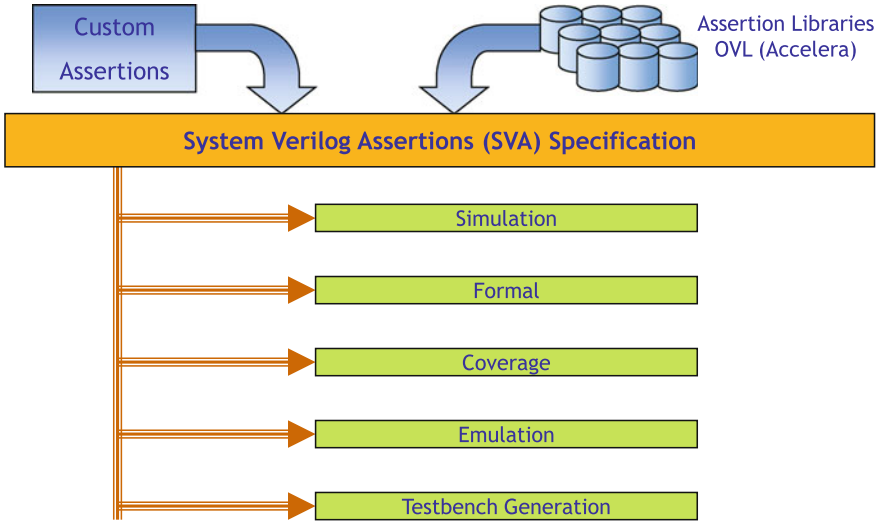


Fig. 2.7 Assertions and OVL for different uses

Figure 2.7 shows the advantage of assertions. Write them once and use them with may tools.

We have discussed at high level the use of assertions in Simulation, Formal, Coverage and Emulation. But how do you use them for Test-bench Generation/Checker and what is OVL assertions library?

Test-bench Generation/Checker: With ever-increasing complexity of logic design, the test benches are getting ever so complex as well. How can assertions help in designing test-bench logic? Let us assume that you need to drive certain traffic to a DUT input under certain condition. You can design an assertion to check for that condition and upon its detection the FAIL action block triggers, which can be used to drive traffic to the DUT. Checking for a condition is far easier with assertions language than with SystemVerilog alone. Second benefit is to place assertions on verification logic itself. Since verification logic (in some cases) is even more complex than the design logic, it makes sense to use assertions to check test-bench logic also.

OVL Library : Open Verification Library. This library of predefined checkers were written in Verilog before PSL and SVA became mainstream. Currently the

library includes SVA (and PSL) based assertions as well. The OVL library of assertion checkers is intended for use by design, integration and verification engineers to check for good/bad behavior in simulation, emulation and formal verification. OVL contains popular assertions such as FIFO assertions, among other. OVL is still in use and you can download the entire standard library from Accellera website: http://www.accellera.org/downloads/standards/ovl.

We will not go into the detail of OVL since there is plenty of information available on OVL on net. OVL code itself is quite clear to understand. It is also a good place to see how assertions can be written for 'popular' checks (e.g. FIFO) once you have better understood assertion semantics.

2.6 Assertions Whining

Maybe the paradigm has now shifted but as of this writing there is still a lot of hesitation on adopting SVA in the overall verification methodology. Here are some popular objections.

- *I don't have time to add assertions. I don't even have time to complete my design. Where am I going to find time to add assertions?*
  - That depends on your definition of "completing my design". If the definition is to simply add all the RTL code without –any- verification/debug features in the design and then throw the design over the wall for verification, your eventual 'working design' will take significantly longer time.
  - During design you are already contemplating and assuming many conditions (state transition assumptions, inter-block protocol assumptions, etc.). Simply convert your assumptions into assertions as you design. They will go a long way in finding those corner case bugs even with your simple sanity test benches.
- *I don't have time to add assertions. I am in the middle of debugging the bugs already filed against my design.*
  - Well, actually you will be able to debug your design in shorter time, if you *did* add assertions as you were designing (or at least add them now) so that if a failing test fires an assertion, your debug time will be drastically short.
  - Assertions point to the source of the bug and significantly reduce time to debug as you verify your block level, chip level design.
  - In other words, this is a bit of chicken & egg problem. You don't have time to write assertions but without these assertions you will spend a lot more time debugging your design!
- *Isn't writing assertions the job of a verification engineer?*
  - Not quite. Design Verification (DV) engineers do not have insight into the micro-architectural level RTL detail. But the real answer is that BOTH

Design and DV engineers need to add assertions. We will discuss that in detail in upcoming section.

- *DV engineer says: I am new to assertions and will spend more time debugging my assertions than debugging the design.*
  - Well, don't you spend time in debugging your test bench logic? Your reference models? What's the difference in debugging assertions? If anything, assertions have proven to be very effective in finding bugs and cutting down on debug time.
  - In my personal experience (over the last many SoC and Processor projects), approximately 25 % of the total bugs reported for a project were DV bugs. There are significant benefits to adding assertions to your test-bench that outweigh the time to debug them.
- *The designer cannot be the verifier also. Doesn't asking a designer to add assertions violate this rule?*
  - As we will discuss in the following sections, assertions are added to check the 'intent' of the design and validate your own assumptions. You are not writing assertions to duplicate your RTL. Following example make it clear that the designer do need to add assertions.
  - For example,

    For every 'req' issued to the next block, I will indeed get an 'ack' and that I will get only 1 'ack' for every 'req'. This is a cross module assumption which has nothing to do with how you have designed your RTL. You are not duplicating your RTL in assertions.
    My state machine should never get stuck in any 'state' (except 'idle') for more than 10 clocks.

2.6.1 Who Will Add Assertions? War Within!

Both Design and Verification engineers need to add assertions…

- Design Engineers:
  - *Micro architectural level decisions/assumptions are not visible to DV engineers*. So, designers are best suited to guarantee uArch level logic correctness.
  - *Every assumption is an assertion*. If you assume that the 'request' you send to the other block will always get an 'ack' in 2 clocks; that's an assumption. So, design and assertion for it.
  - *Add assertions as you design your logic, not as an afterthought*.

- DV Engineers:
  - *Add assertions to check macro functions and Chip/SoC level functionality.*

    Once the packet has been processed for L4 layer, it will indeed show up in the DMA queue.
    A machine check exception indeed sets PC to the exception handler address.

  - *Add assertions to check Interface IO logic*

    After Reset is de-asserted none of the signals ever go 'X'.
    If the processor is in Wait Mode and no instructions are pending that it must assert a SleepReq to memory subsystem within 100 clocks.
    On Critical Interrupt, the external clock/control logic block must assert CPU_wakeup within 10 clocks.

2.7 A Simple PCI Read Example: Creating an Assertions Test Plan

Let us consider a simple example of PCI Read. Given the specification in Fig. 2.8, what type of assertions would the design team add and what type would the verification team add? The tables below describe the difference. I have only given few of the assertions that could be written. There are many more assertions that need to be written by verification and design engineers. However, this example will act as a basis for differentiation.

Designers add assertions at micro-architecture level while verification engineers concentrate at system level, specifically the interface level in this example.

We will model the assertions for this PCI protocol later in the book under LAB6 exercise. It is too early to jump into writing assertions without knowing the basics at this stage.

The PCI protocol is for a simple READ. With FRAME_ assertion, AD address and C_BE_ have valid values. Then IRDY_ is asserted to indicate that the master is ready to receive data. Target transfers data with intermittent wait states. Last data transfer takes place a clock after FRAME_ is de-asserted.

Let us see what type of assertions need to be written by design and verification engineers (Tables 2.1 and 2.2).

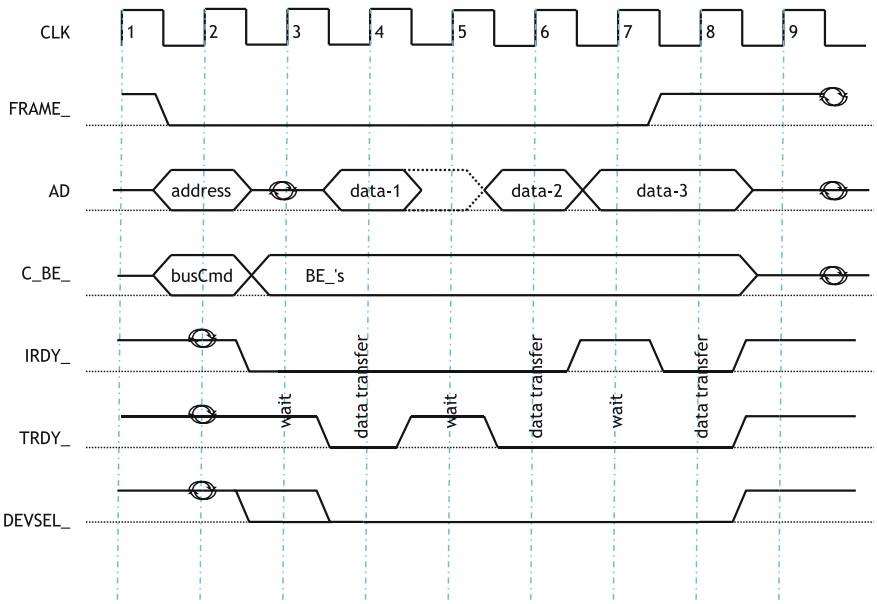


Fig. 2.8 A simple PCI read protocol

Table 2.1 PCI read protocol test plan by functional verification team

Property name	Description	Property fail?	Property covered?
Protocol interface assertions			
checkpci_AD_CBE (check1)	On falling edge of FRAME_, AD and C_BE_ bus cannot be unknown		
checkpci_DataPhase (check2)	When both IRDY_ and TRDY_ are asserted, AD or C_BE_ bus cannot be unknown		
checkPCI_Frame_Irdy (check3)	FRAME can be de-asserted only if IRDY_ is asserted		
checkPCI_trdyDevsel (check4)	TRDY_ can be asserted only if DEVSEL_ is asserted		
checkPCI_CBE_during_trx (check5)	Once the cycle starts (i.e. at FRAME_ assertion) C_BE_ cannot float until FRAME_ is de-asserted		

Table 2.2 PCI read protocol test plan by design team

Property name	Description	Property fail?	Property covered?
Microarchitectural Assertions			
check_pci_adrcbe_St	PCI state machine is in 'adr_cbe' state the first clock edge when FRAME_ is found asserted		
check_pci_data_St	PCI state machine is in 'data_transfer' state when both IRDY_ and TRDY_ are asserted		
check_pci_idle_St	PCI state machine is in 'idle' state when both FRAME_ and IRDY_ are de-asserted		
check_pci_wait_St	PCI state machine is in 'wait' state if either IRDY_ or TRDY_ is de-asserted		

Note that in the table there are two columns. (1) Did the property FAIL? (2) Did the property get covered? There is no column for the property PASS. That is because, 'cover' in an assertion triggers only when a property is exercised but does not fail; in other words it passes. Hence, there is no need for a PASS column. This 'cover' column tells you that you indeed covered (exercised) the assertion and that it did not fail. When the assertion FAILs, it tells you that the assertion was exercised (covered) and that it Failed during the exercise.

2.8 What Type of Assertions Should I Add?

It is important to understand and plan for the types of assertions one needs to add. Make this part of your verification plan. It will also help you partition work among your team.

Note the 'performance implication' assertions. Many miss on this point. Coming from processor background, I have seen that these assertions turn out to be some of the most useful assertions. These assertions would let us know of the (e.g.) cache read latency upfront and would allow us enough time to make architectural changes.

- RTL Assertions (design intent)
  - Intra Module;

    Illegal state transitions; deadlocks; livelocks;
    FIFOs, onehot, etc.
- Module interface Assertions (design interface intent)
  - Inter-module protocol verification; illegal combinations (ack cannot be '1' if req is '0'); steady state requirements (when slave asserts write_queue_full, master cannot assert write_req);
- Chip functionality Assertions (chip/SoC functional intent)
  - A PCI transaction that results in Target Retry will indeed end up in the Retry Queue.
- Chip interface Assertions (chip interface intent)
  - Commercially available standard bus assertion VIPs can be useful in comprehensive check of your design's adherence to std. protocol such as PCIX, AXI, etc.
  - Every design assumption on IO functionality is an assertion.
- Performance Implication assertions (performance intent)
  - Cache latency for read; packet processing latency; etc. to catch performance issues before it's too late. This assertion works like any other. For example, if the 'Read Cache Latency' is greater than 2 clocks, fire the assertion. This is an easy to write assertion with very useful return.

2.9 Protocol for Adding Assertions

- Do not duplicate RTL
  - White box observability does not mean adding an assertion for each line of RTL code. This is a very important point, in that if RTL says 'req' means 'grant', don't write an assertion that says the same thing!! Read on.
  - Capture the intent

    For example, a Write that follows a Read to the same address in the request pipe will always be allowed to finish before the Read. This is the intent of the design. How the designer implements reordering logic is not of much interest. So, from verification point of view, you need to write assertions that verify the chip specifications.
    A note here that the above does not mean you do not add low-level assertions. Classic example here is FIFO assertions. Write FIFO assertions for all FIFOs in your design. FIFO is low-level logic, but many of the critical bugs hang around FIFO logic and adding these assertions will provide maximum bang for your buck.
- Add assertions throughout the RTL design process
  - They are hard to add as an after-thought.
  - Will help you catch bugs even with your simple block level test bench.
- If an assertion did not catch a failure.
  - If the test failed and none of the assertions fired, see if there are assertions that need to be added which would fire for the failing case.
  - The newly added assertion is now active for any other test that may trigger it. Note: This point is very important towards making a decision if you have added enough assertions. In other words, if the test failed and none of the assertions fired, there is a good chance you still have more assertions to add.
- Reuse
  - Create libraries of common 'generic' properties with formal arguments that can be instantiated (reused) with 'actual' arguments. We will cover this further in the book.
  - Reuse for the next project.

2.10 How do I Know I have Enough Assertions?

- It's the "Test plan, test plan, test plan…"
  - Review and re-review your test plan against the design specs.
  - Make sure you have added assertions for every 'critical' function that you must guarantee works.

- If tests keep failing but assertions do not fire, you do not have enough assertions.
  - In other words, if you had to trace a bug from primary outputs (of a block or SoC) without any assertions firing that means that you did not put enough assertions to cover that path.
- 'formal' (aka static formal aka static functional verification) tool's ability to handle assertions
  - What this means is that if you don't have enough 'assertion density' (meaning if a register value does not propagate to an assertion within 3 to 5 clocks—resulting in assertions sparsely populated within design), the formal analysis tool may give up on the state/space explosion problem. In other words, a static functional formal tool may not be able to handle a large temporal domain. If the assertion density is high, the tool has to deal with smaller cone of logic. If the assertion density is sparse, the tool has to deal with larger cone of logic in both temporal and combinatorial space and it may run into trouble.

2.11 Use Assertions for Specification and Review

- Use assertions (properties/sequences) for specification
  - DV (Design Verification) Team:

    Document as much of the 'response checking' part of your test plan as practical directly into executable properties.
    Use it for verification plan review and update
  - Design Team:

    Document micro-arch. level assertions directly into executable properties.
    Use it for design reviews.
- Assertions Cross-Review
  - Review:

    DV team reviews macro, chip, interface level assertions with the design team.
  - Cross Review

    Block A designer reviews module B interface assertions
    Block B designer reviews module A interface assertions
  - Mis-assumptions, incorrect communication are detected early on.

2.12 Assertion Types

There are three kinds of assertions supported by SVA. In brief, here's their description. We will discuss them in plenty detail throughout this book.

- Immediate Assertion
- Concurrent Assertion
- Deferred Assertion (introduced in IEEE 1800-2009)

Immediate Assertions

- Simple *non-temporal domain assertions* that are executed like statements in a procedural block,
- Interpreted the same way as an expression in the conditional of a procedural 'if' statement
- Can be specified only where a procedural statement is specified.

Concurrent Assertions

- These are *temporal domain assertions* that allow creation of complex sequences using clock (sampling edge) based semantics.
- They are edge sensitive and not level sensitive. In other words, they must have a 'sampling edge' on which it can sample the values of variables used in a sequence or a property.

Deferred Assertions (introduced in IEEE 1800-2009)

- Deferred assertions are a type of Immediate assertions. Note that immediate assertions evaluate immediately without waiting for variables in its combinatorial expression to *settle* down. This also means that the immediate assertions are very prone to glitches as the combinatorial expression settles down and may fire multiple times. On the other hand, deferred assertions do not evaluate their sequence expression until the end of time stamp when all values have settled down (or in the reactive region of the time stamp).

If some of this does not quite make sense, which is OK. That is what the rest of the book will explain. Let us start with Immediate assertions and understand its semantics. We then move on to Concurrent assertions and lastly Deferred assertions. The book focuses on concurrent assertions because that is really the main gist of SystemVerilog Assertion Language.

2.13 Conventions Used in the Book

Table 2.3 Conventions used in this book

	LEVEL SENSITIVE HIGH: This symbol means that the signal is detected HIGH (level sensitive) at the clock edge noted in a timing diagram. It could have been high or low the previous clock and may remain high or low after the clock edge. *It does NOT however mean that a 'posedge' is expected on this signal at the noted clock edge*
	LEVEL SENSITIVE LOW: This symbol means that the signal is detected LOW (level sensitive) at the clock edge noted in a timing diagram. It could have been high or low the previous clock and may remain high or low after the clock edge. *It does NOT however mean that a 'negedge' is expected on this signal at the noted clock edge*
	EDGE SENSITIVE HIGH: This symbol means that a posedge is expected on this signal
	EDGE SENSITIVE LOW: This symbol means that a negedge is expected on this signal
	PROPERTY PASSes: This symbol means that a sequence/property match is detected here (i.e. the sequence/property PASSes)
	PROPERTY FAILs: This symbol means that a sequence/property did not match here (i.e. the sequence/property FAILs)

Note that the level sensitive attribute of a signal is shown as a 'fat' High and Low symbol. I could have drawn regular timing diagrams but saw that they look very cumbersome and does not easily convey the point. Hence, I chose the fat arrow to convey that ***when the fat arrow is high, the signal was high before the clock; at the clock and after the clock. The same applies for the fat low arrow.***

For edge sensitive assertions, I chose the regular timing diagram to distinguish them from the level sensitive symbol.

A high (thin) arrow is for PASS and a low (thin) arrow is for FAIL (Table 2.3).

Chapter 3
Immediate Assertions

Immediate assertions are simple non-temporal domain assertions that are executed like statements in a procedural block. Interpret them as an expression in the condition of a procedural 'if' statement. Immediate assertions can be specified only where a procedural statement is specified.

Figure 3.1 describes the basics of an immediate assertion. It is so called because it executes immediately at the time it is encountered in the procedural code. It does

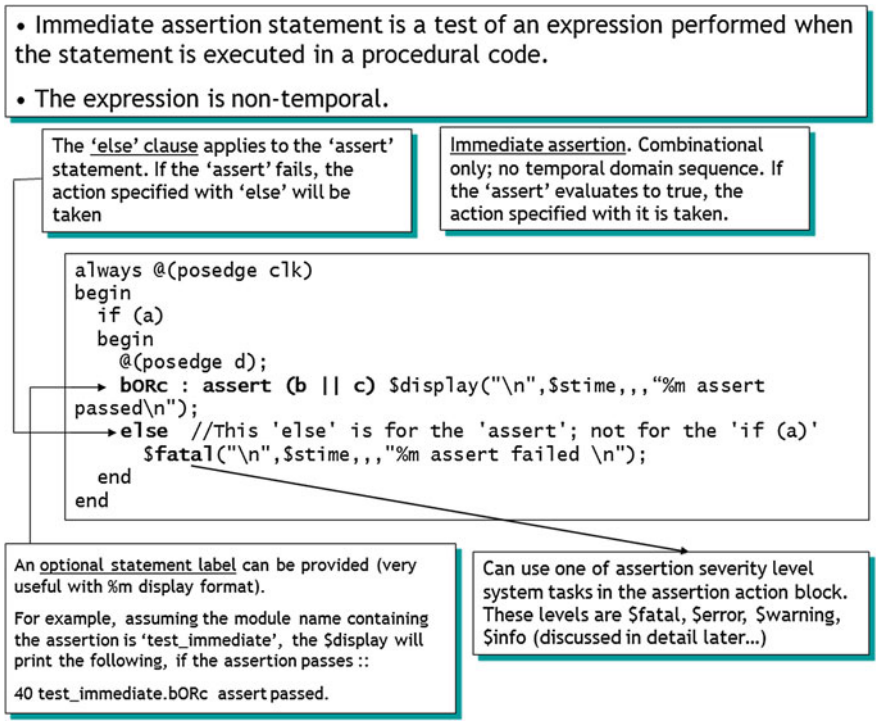


Fig. 3.1 Immediate Assertion—Basics

A. B. Mehta, *SystemVerilog Assertions and Functional Coverage*,
DOI: 10.1007/978-1-4614-7324-4_3,

not wait for the 'next clock edge' to fire itself. The assertion can be preceded by a level sensitive or an edge sensitive statement. As we will see that concurrent, assertions can only work on a 'sampling/clock edge' sensitive logic and not level sensitive logic.

We see in Fig. 3.1 that there is an immediate assertion embedded in the procedural block that is triggered by @ (posedge clk). The immediate assertion is triggered after @ (posedge d) and checks to see that (b || c) is true.

We need to note a couple of points here. First, the very preceding statement in this example is @ (posedge d), an edge sensitive statement. However, it does not have to be. It can be a level sensitive statement also or any other procedural statement. The reason I am pointing this out is that concurrent assertions can work only off of a sampling 'edge' and not off of a level sensitive control. Keep this in your back pocket because it will be very useful to distinguish immediate assertions from concurrent assertions when we cover the latter. Second, the assertion itself cannot have temporal domain sequences. In other words, an immediate assertion cannot consume 'time'. It can only be combinatorial which can be executed in zero time. In other words, the assertion will be computed and results will be available at the *same* time that the assertion was fired. If the 'assert' statement evaluates to 0, X, Z then the assertion will be considered to be a FAIL else it will be considered to be a PASS.

We also see in the figure that there is (what is known as) an Action Block associated with FAIL or PASS of the assertion. This is no different than the PASS/FAIL logic we are used to design for an 'if..else' statement.

From syntax point of view, an immediate assertion uses only "assert" as the keyword in contrast to a concurrent assertion that requires "assert property".

One key difference between immediate and concurrent assertions is that concurrent assertions always work off of the sampled value in preponed region of a simulation tick while immediate assertions work immediately when they are executed (as any combinatorial expression in a procedural block) and do not evaluate its expression in the preponed region. Keep this thought in your back pocket for now since we have not yet seen concurrent assertions and how assertions get evaluated in a simulation time tick. But this key difference will become important to note as you learn more about concurrent assertions.

Finally, as we discussed above, the immediate assertion works on a combinatorial expression whose variables are evaluated 'immediately' at the time the expression is evaluated. These variables may transition from one logic value to another (e.g. 1 to 0 to 1) within a given simulation time tick and the immediate assertion may get evaluated multiple times before the expression variable values 'settle' down. This is why immediate assertions are also known to be 'glitch' prone.

To complete the story, there are three types of immediate assertions.

immediate **assert**
immediate **assume**
immediate **cover**

'**assume**' and '**cover**' are too early to discuss. We will discuss those as part of concurrent assertions. The most useful is the 'immediate **assert**' which is what we have discussed here.

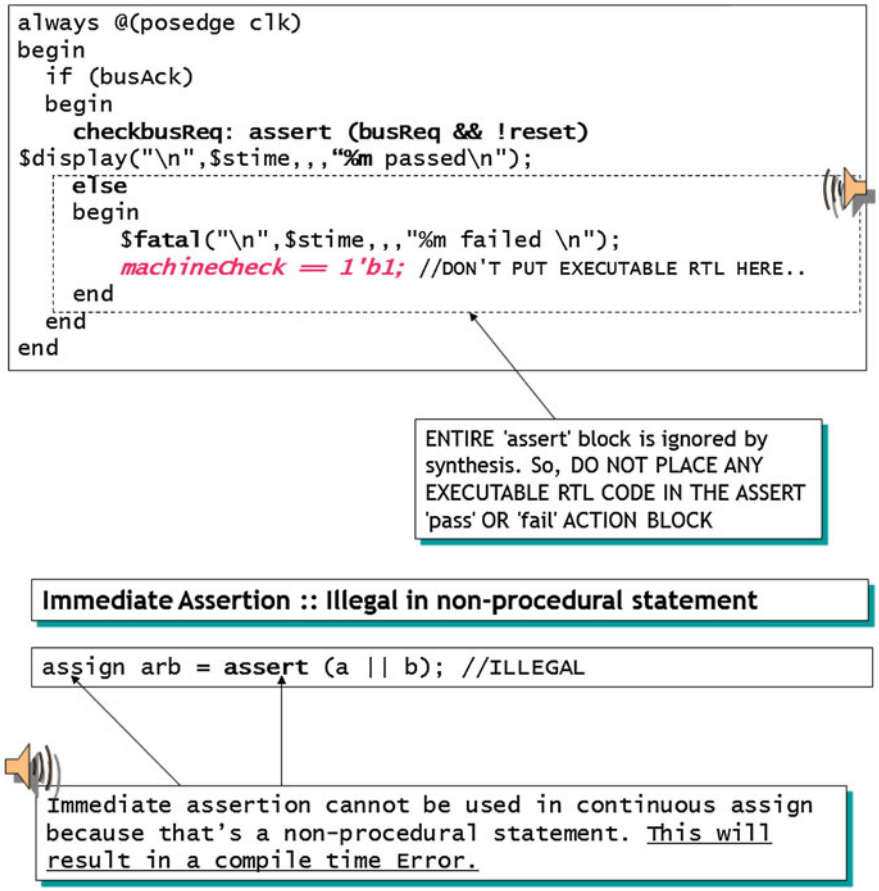


Fig. 3.2 Immediate Assertions: Finer points

Figure 3.2 points out a couple of finer points. First, do not put anything in the so-called action block (PASS or FAIL) of the immediate assertion. Most synthesis tools will simply ignore the entire immediate assertion with its action blocks (which makes sense) and with it will go your logic that (if) you were planning on putting in your design. This is rather obvious but easy to miss.

Note that an immediate assertion cannot be used in a continuous assignment statement because continuous assign is not a procedural block. Lastly, please note that IEEE-1800 2009 LRM also defines another type of immediate assertion, which is called Deferred Assertion. We will discuss deferred assertion under the chapter solely devoted to IEEE-1800 2009 features for assertions.

Chapter 4
Concurrent Assertions: Basics (Sequence, Property, Assert)

These are temporal domain assertions that allow creation of complex sequences using *clock* (*sampling*) *edge* based semantics. This is in contrast to the immediate assertions that are purely combinatorial and do not allow temporal domain sequences.

Concurrent assertions are the gist of SVA language. They are called concurrent because they execute in parallel with the rest of the design logic. Let us start with basics and move onto the complex concepts of concurrent assertions.

Let us first learn the basic syntax of a concurrent assertion and then study it's semantics.

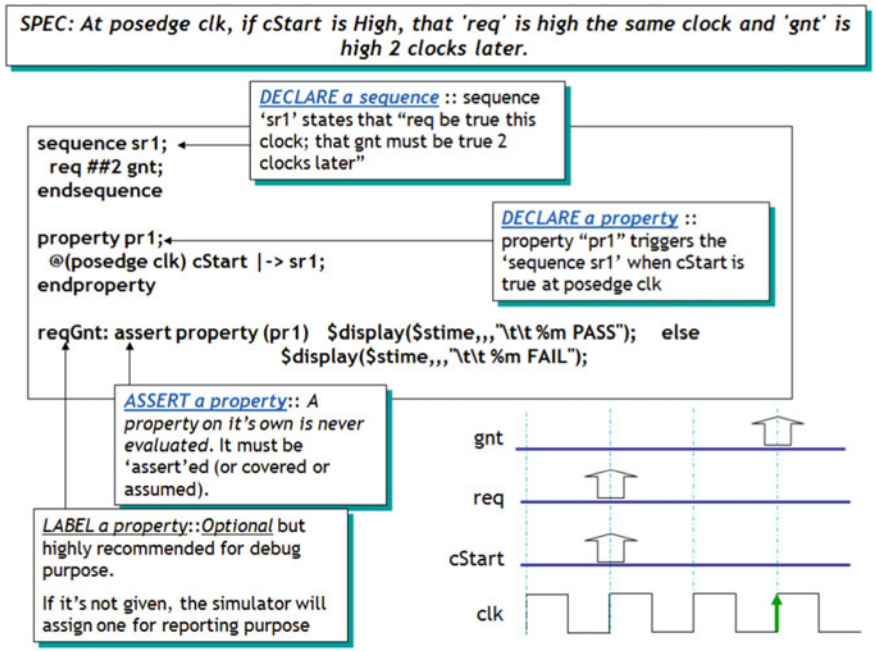


Fig. 4.1 Concurrent assertion—basics

A. B. Mehta, *SystemVerilog Assertions and Functional Coverage*,
DOI: 10.1007/978-1-4614-7324-4_4,

In Fig. 4.1 we have declared a property 'pr1' and asserted it with a label 'reqGnt' (label is optional but highly recommended). The figure explains various parts of a concurrent assertion including a property; a sequence and assertion of the property.

The 'assert property (pr1)' statement triggers property 'pr1'. 'pr1' in turn waits for the antecedent 'cStart' to be true at a (posedge clk) and on it being true implies (fires) a sequence called 'sr1'. 'sr1' checks to see that 'req' is high when it is fired and that 2 'clocks' later 'gnt' is true. If this temporal domain condition is satisfied then the sequence 'sr1' will PASS and so will property 'pr1' and the 'assert property' will be a PASS as well. Let us continue with this example and study other key semantics.

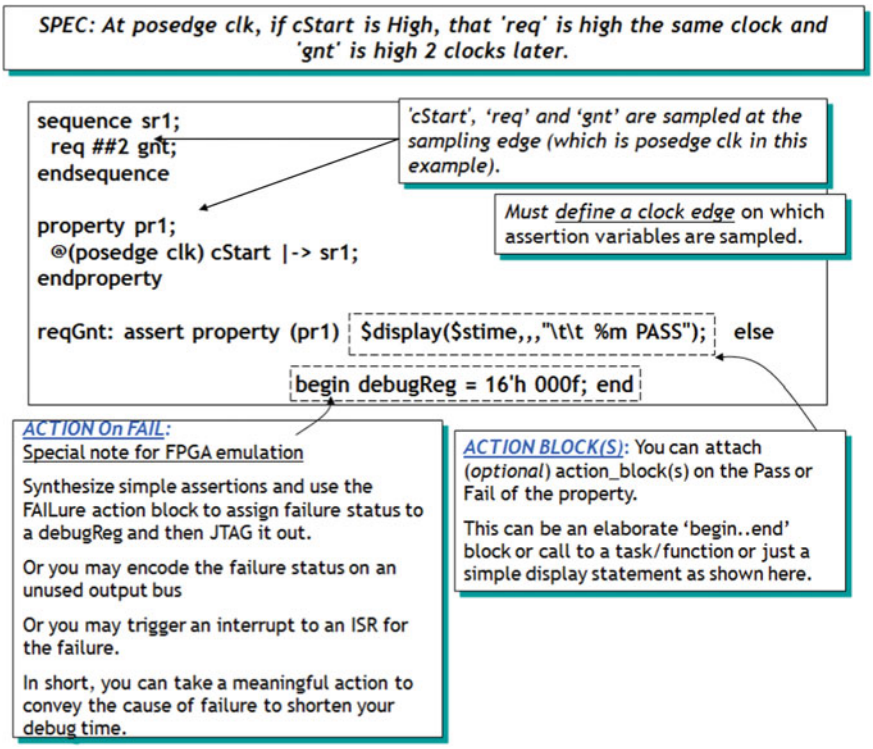


Fig. 4.2 Concurrent assertion—sampling edge and action blocks

As explained in Fig. 4.2, following are the basic and mandatory parts of an assertion. Each of these features will be further explored as we move along.

(1) 'assert'—you have to assert a property; i.e., invoke or trigger it.
(2) There is an action block associated with either the pass or fail of the assertion
(3) 'property pr1' is edge triggered on posedge of clk (more on the fact that you *must* have a sampling edge for trigger is explained further on).
(4) 'property pr1' has an *antecedent* which is a signal called cStart, which if sampled high (in the preponed region) on the posedge clk, will imply that the *consequent* (sequence sr1) be executed.

(5) Sequence sr1 samples 'req' to see if it is high exactly at the time it was triggered (i.e., the same posedge of clk when the sequence was triggered because of the *overlapping implication* operator) and then waits for 2 clks and sees if 'gnt' is high.
(6) Note that each of 'cStart', 'req', 'gnt' are sampled at the edge specified in the property which is the posedge of 'clk'. In other words, even though there is no edge specified in the sequence, the edge is inherited from property pr1.

Note also that we are using the notion of sampling the values at posedge clk which means that the 'posedge clk' is the '*sampling edge*'. In other words, the sampling edge can be anything (as long as it's an edge and not level sensitive), meaning it does not necessarily have to be a synchronous edge such as a clock. It can be an asynchronous edge as well. However, *be very careful about using an asynchronous edge* unless you are sure what you want to achieve. I have devoted a complete example on the pitfalls of using an asynchronous edge as the sampling edge. It's too soon to get into. This is a very important concept in concurrent assertions and should be well understood. However, do not worry, you will get much more insight as we move further.

Now, let us slightly modify the sequence 'sr1' to highlight boolean expression in a sequence or a property and study some more key elements of a concurrent assertion.

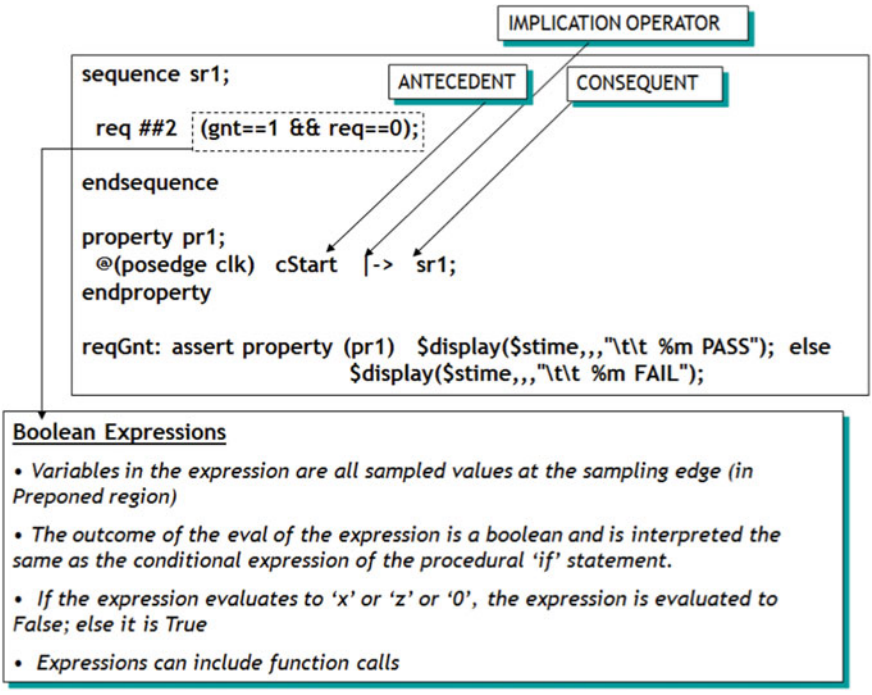


Fig. 4.3 Concurrent assertion—implication, antecedent and consequent

As shown in Fig. 4.3 there are three main parts of the expression that determines when an assertion will fire, what will it do once fired and time duration between the firing event and execution event.

The condition under which an assertion will be fired is called an '*antecedent.*' This is the LHS of the implication operator.

RHS of the assertion that executes once the antecedent matches is called the '*consequent*'

The '*implication*' operator determines the time duration that will lapse between the antecedent and the consequent. In other words, the implication operator ties the antecedent and the consequent in one of two ways. It ties them with an '*overlapping*' implication operator or a '*non-overlapping*' implication operator. The way to 'read' the implication operator is "if there is a match on the antecedent that the consequent will be executed. If there is no match, consequent will not fire and the assertion will continue to wait for a match on the antecedent".

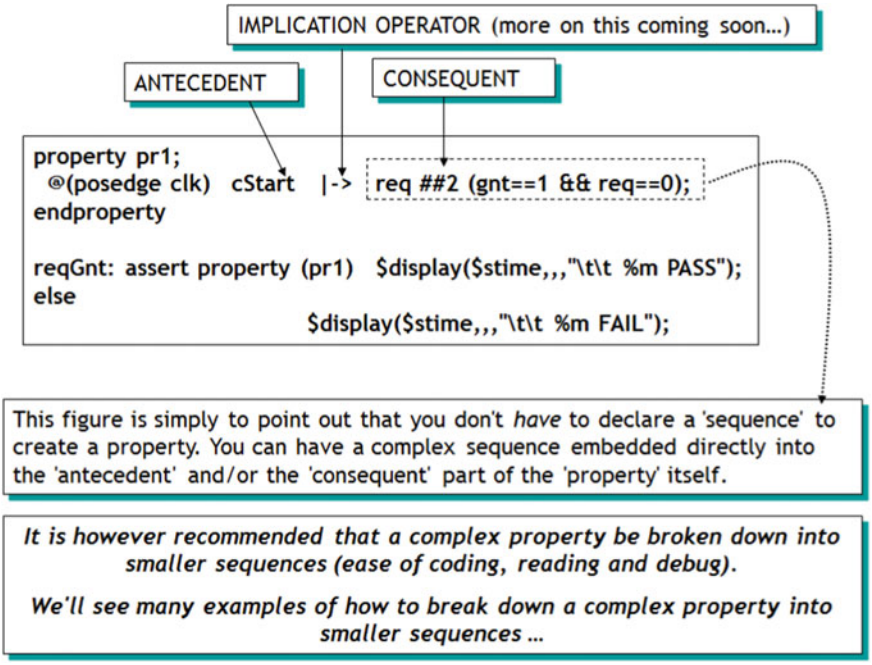


Fig. 4.4 Property with an embedded sequence

Figure 4.4 further explains the antecedent and consequent. As shown, you donot have to have a sequence in order to model a property. If the logic to execute in consequent is simple enough then it can be declared directly in consequent as shown. But please note that it is always best to break down a property into smaller sequences to model complex properties/sequences. Hence, consider this example only as describing the semantics of the language. Practice should be to divide and

conquer. You will see many examples, which seem very complex to start with, but once you break them down into smaller chunks of logic and model them with smaller sequences, tying all those together will be much easier then writing one long complex assertion sequence.

4.1 Implication Operator, Antecedent and Consequent

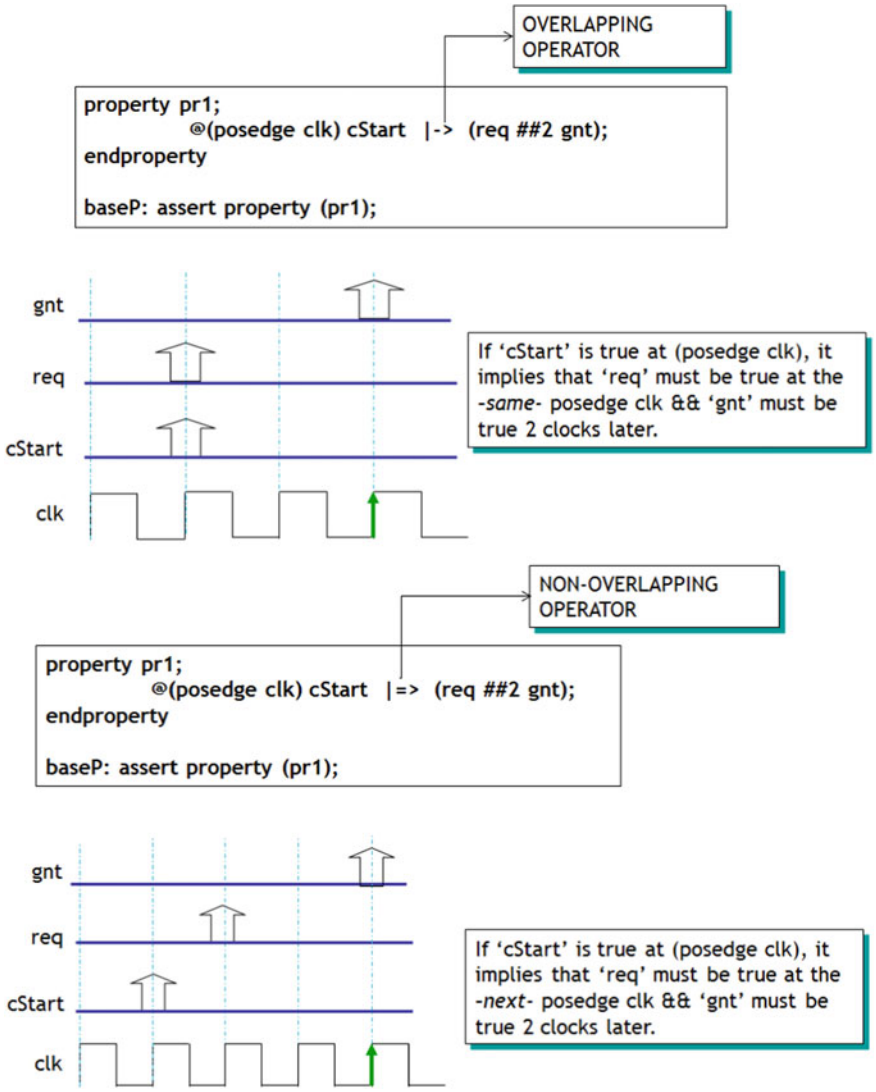


Fig. 4.5 Implication operator—overlapping and non-overlapping

Implication operator ties the antecedent and consequent. If antecedent holds true it implies that the consequent should hold true.

There are two types of implication operators as shown in Fig. 4.5.

(1) Overlapping Implication Operator: Referring to Fig. 4.5, the top most property shows the use of an overlapping operator. Note its symbol (|->), which differs from that of the non-overlapping operator (|=>). Overlapping means that when the antecedent is found to be true, that the consequent will start it is execution (evaluation) the '*same*' clk. As shown in the figure, when cStart is sampled High at posedge of clk that the req is required to be High at the 'same' posedge clk. This is shown in the timing diagram associated with the property.

   a. So, what happens if 'req' is sampled true at the next posedge clk after the antecedent (and false before that)? Will the overlapping property pass?

(2) Non-Overlapping Implication Operator: In contrast, non-overlapping means that when the antecedent is found to be true that the consequent should start it is execution, one clk *later*. This is shown in the timing diagram associated with the property.

   a. So, what happens if 'req' is sampled true at the same posedge clk as the antecedent (and False after that)? Will the non-overlapping property pass?

Answer to both 1.a and 2.a is NO.

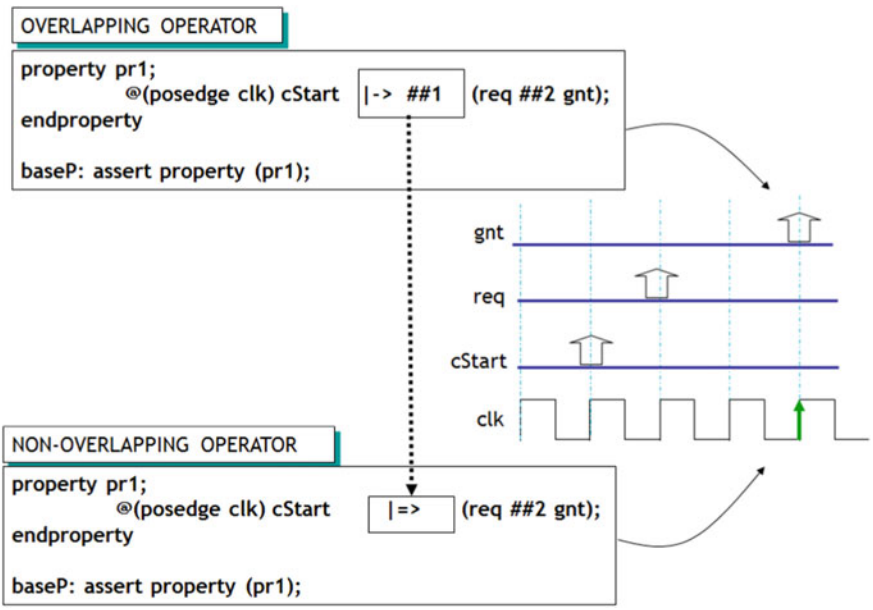


Fig. 4.6 Equivalence between overlapping and non-overlapping implication operators

Figure 4.6 further shows the equivalence between overlapping and non-overlapping operators. '|=>' is equivalent to '|-> ##1'. Note that ##1 is not the same as Verilog's #1 delay. ##1 means one clock edge (sampling edge). Hence '|-> ##1' means the same as '|=>'.

Suggestion: To make debugging easier and have project wide uniformity, use the overlapping operator in your assertions. Reason? Overlapping is the common denominator of the two types of operator. You can always model non-overlapping from overlapping and but you cannot do vice versa. What this means is that during debug everyone would know that all the properties are modeled using overlapping and that the # of clocks are exactly the same as specified in the property. You do not have to add or subtract from the # of clocks specified in the chip specification. More important, if everyone uses his or her favorite operator, debugging would be very messy not knowing which property uses which operator.

4.2 Clocking Basics

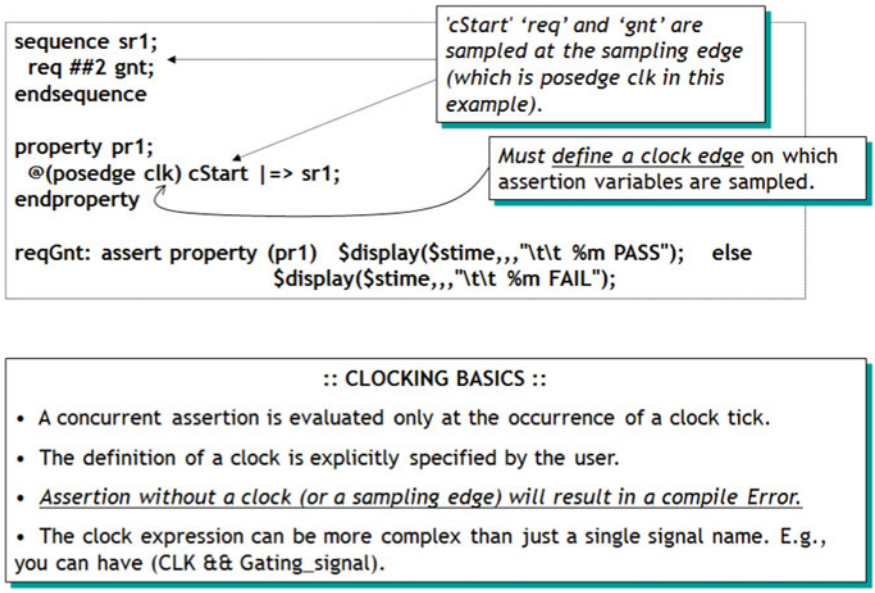


Fig. 4.7 Clocking basics

As mentioned before, a concurrent assertion is evaluated only on the occurrence of an 'edge', known as the 'sampling edge'. The reason for continually mentioning this 'edge' as 'clk' is because it is best to have this 'edge' synchronous to either posedge or negedge for a signal. You can indeed have an asynchronous edge as well. BUT be very careful. I have devoted a complete example precisely to explain

how an assertion with an asynchronous edge works. It gets—very—complicated and I highly discourage you from writing one unless you are absolutely sure you know what you are doing. In Fig. 4.7, we are using a non-overlapping implication operator, which means that at a posedge of clk if cStart is high, then one clock later sr1 should be executed.

Let us revisit 'sampling' of variables. The expression variables cStart, req and gnt are all sampled in the *preponed region* of posedge clk. In other words, if (e.g.) cStart = 1 and posedge clk changed at the same time, the sampled value of cStart in the preponed region will be equal to 'zero' and not 'one'. We will soon discuss what 'preponed region' really means in a simulation time tick and how it affects the evaluation of an assertion, especially when the sampling edge and the sampled variable change at the same time.

Note again that 'sequence sr1' does not have a clock in its expression. The clock for 'sequence sr1' is inherited from the 'property pr1'. This is explained next using Fig. 4.8.

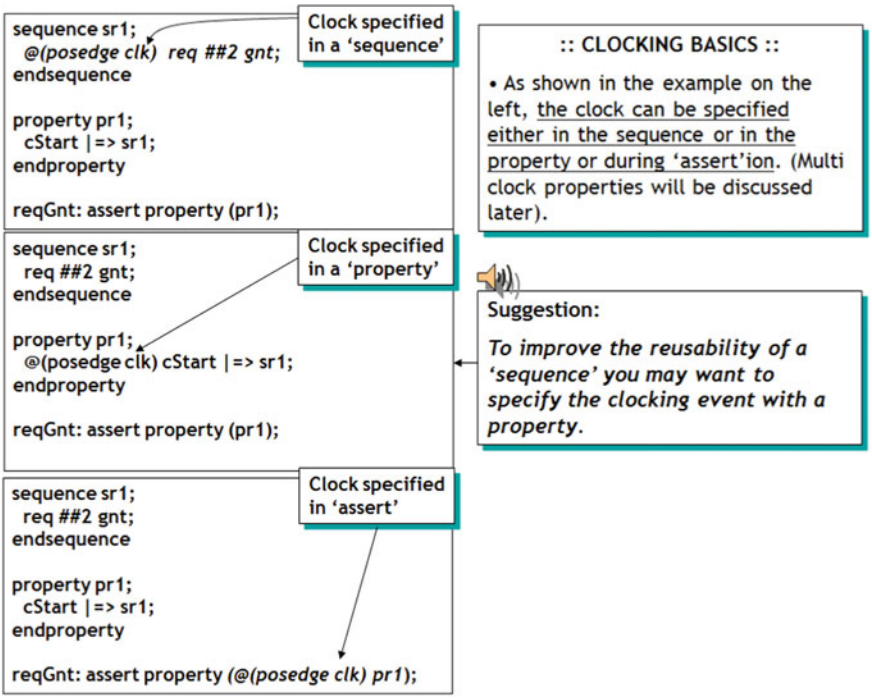


Fig. 4.8 Clocking basics—clock in 'assert', 'property' and 'sequence'

As explained in Fig. 4.8, the 'clk' as an edge can be specified either directly in the assert statement or in the property or in the sequence. Regardless of where it is declared, it will be inherited by the entire assertion (i.e. the assert, property and sequence blocks).

Suggestion: As noted in the Fig. 4.8, my recommendation is to specify the 'clk' in a property. Reason being you can keep sequences void of sampling edge (i.e., 'clk') and thus make them reusable. The sampling edge can change in the property but sequence (or cascaded sequences) remain untouched and can change their logic without worrying about the sampling edge. Note that it is also more readable when the sampling edge 'clk' is declared just before the antecedent in a property. "At posedge of clk, if cStart is high, trigger sr1".

4.3 Sampling Edge (Clock Edge) Value: How are Assertions Evaluated in a Simulation Time Tick?

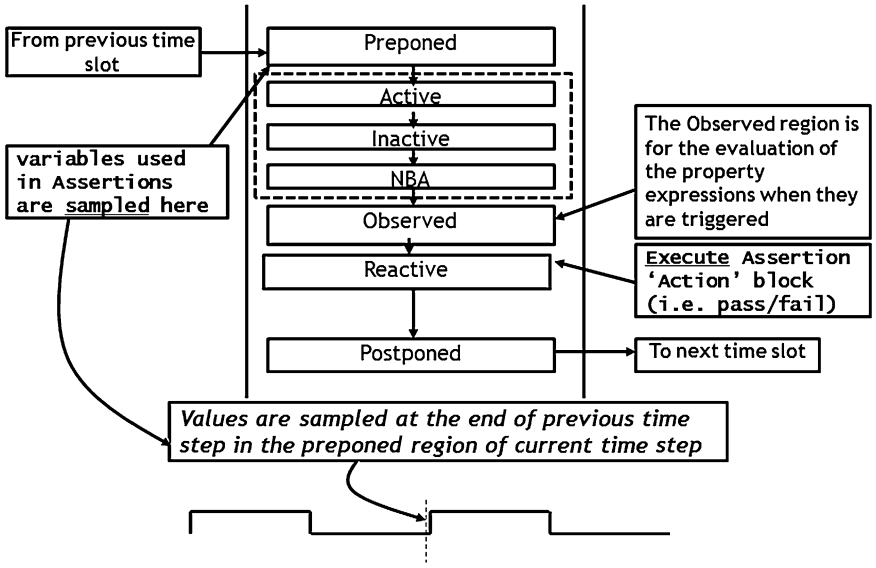


Fig. 4.9 Assertions variable sampling and evaluation/execution in a simulation time tick

How does the so-called sampling edge sample the variables in a property or a sequence is one of the most important concept you need to understand when designing assertions. As shown in Fig. 4.9 the important thing to note is that the variables used in assertions (property/sequence/expression) are sampled in the '*preponed*' region. What does that mean? It means (for example) if a sampled variable changes the same time as the sampling edge (e.g. clk) that the value of the variable will be the value it held—*before*—the clock edge.

@ (posedge clk) a |=> !a;

In the above sequence, let us say that variable 'a' changes to '1' the same time that the sampling edge clock goes posedge clk (and assume 'a' was '0' before it went to a '1'). Will there be a match of the antecedent 'a'? No! Since a' went from '0' to '1' the same time that clock went posedge clk, the value of 'a' sampled by clock will be '0' (preponed region) and not '1'. This will not cause the property to trigger because the antecedent is not evaluated to be true. This will confuse you during debug. You would expect '1' to be sampled and the property triggered thereof. However, you will get just the opposite result.

This is a very important point to understand because in a simulation waveform (or for that matter with Verilog $monitor or $strobe) you will see a '1' on 'a' with posedge clk and would not understand why the property did not fire or why it failed (or passed for that matter). Always remember that at the sampling edge, the 'previous' value (i.e. a delta before the sampling edge in the preponed region) of the sampled variable is used.

Here is a complete example including the test-bench and comments that explain how sampling of variables in the preponed region affects assertion results.

```
module assert1;

reg A, B, C, D, clk;

property ab;

  @ (posedge clk) !A |-> B;

endproperty

aba: assert property (ab) else $display($stime,,, "ab FAIL");

abc: cover property (ab) $display($stime,,, "ab PASS");


initial begin

  clk = 0; A = 0; B = 0; //Note: A and B are equal to '0' at time 0.


  forever #10 clk = !clk;

end

initial begin

'ifdef PASS

/* Following sequence of events will cause property 'ab' to PASS because even
though A = 0 and B = 1 change simultaneously they had settled down because of
#1 before posedge clk. Hence when @ (posedge clk) samples A, B; A = 0 and
B = 1 are sampled. The property antecedent '!A' is evaluated to be true and at that
same time (overlapping operator) B == 1. Hence the property passes */
```

```
A = 0;
B = 1;
#1;
@ (posedge clk)
‘else
/* Following sequence of events will cause property ‘ab’ to FAIL. Here’s the story.
A = 0 and B = 1 change at the same time as posedge clk. This causes the sampled
value of B to be equal to ‘0’ and not ‘1’ because the sampling edge (posedge clk)
samples the variable values in the preponed region and B was equal to ‘0’ in the
preponed region. Note that A was equal to ‘0’ in the preponed region because of its
initialization in the ‘initial’ block above. So, now you have both ‘A’ and ‘B’ == 0.
Since A is 0, !A is true and the property evaluation takes place. Property expects
B == 1 the same time (overlapping operator) that !A is true. However, ‘B’s
sampled value is ‘0’ and the property fails. */
  @ (posedge clk)
  A = 0;
  B = 1;
‘endif
@ (negedge clk)
$finish(2);
end
endmodule
```

4.3.1 Default Clocking Block

For a long chain of properties and sequences in the file, you can also use the default clocking block as explained in the Fig. 4.10. The figure is self-explanatory in the different ways in which clocking block can be declared and the scope in which it is effective. The top block of the figure shows declaration of ‘default clocking cb1’ which is then inherited by the properties ‘checkReqGnt’ and ‘checkBusGrant’ that follow. This default clocking block will be in effect until another default clocking block is defined. The bottom part of the figure is interesting. Here the properties are directly embedded in the default clocking block. I donot recommend doing that though. The clocking block should only contain clock specifications, which will keep it modular and reusable. Use your judgment call wisely on such issues.

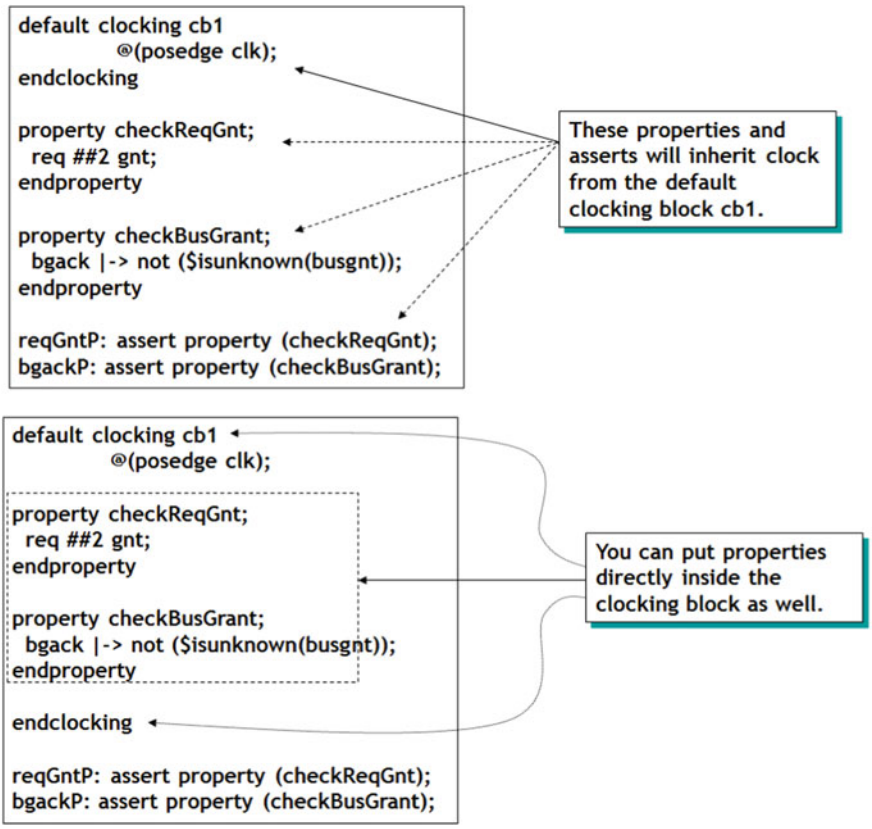


Fig. 4.10 Default clocking block

Figure 4.11 declares two clocking blocks, namely 'cb1' and 'cb2' in a stand-alone Verilog module called 'design_clocks'. This is a great way to organize your clocking strategy in one module. Once defined, you can use any of the clocking block that is required simply by referring to it by its hierarchical instance name as shown in the figure.

Here is some food for thought. I have outlined a couple of pros and cons of using a default-clocking block. It is mostly advantageous but there are some caveats.

Pros: The argument towards default block is reusability. You may change the clocking relation in the default block and it will be applicable to all the following blocks. You do not have to individually change clocking scheme in each property. This is indeed a true advantage and if you plan to change the clocking scheme in the default block without affecting the properties that follow, do use the default block by all means.

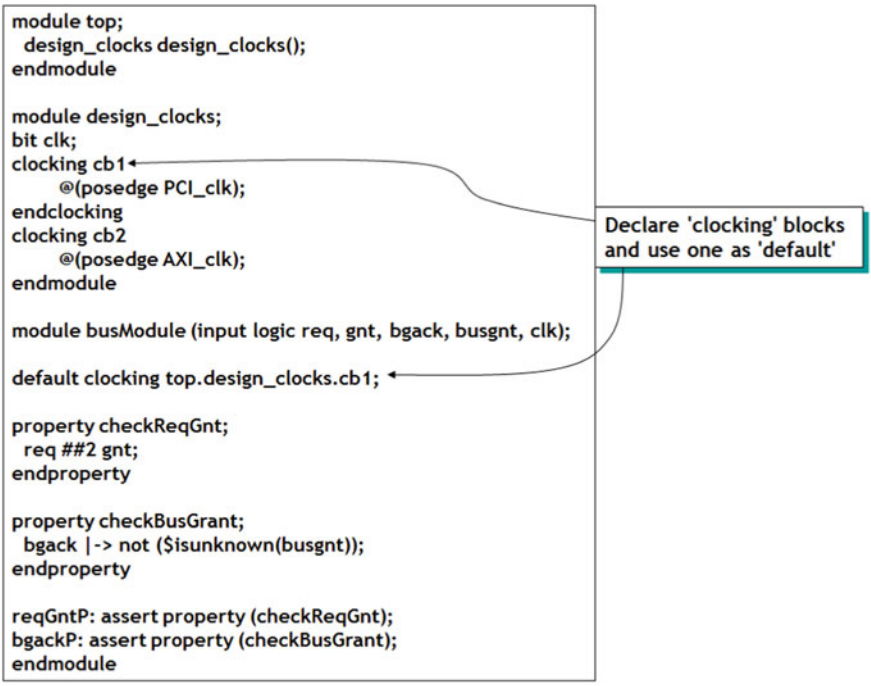


Fig. 4.11 'Clocking' and 'default clocking'

Cons: Readability/debuggability: When you see a property without any sampling edge, you have to scroll back to 'someplace' above the property to see what sampling edge is being used. You have to find the very preceding clocking block and cannot just go to the top of the file. I like properties that are mostly self-contained with the sampling edge. Sure, it is a bit more typing but a lot more readable.

4.3.2 Gated Clk

Figure 4.12 shows an interesting modeling application of using a gated clk as the sampling edge for a property. Note that assign is out of the scope of assertion. But it is assigned value 'clkstart' can indeed be used in the property. In general, any variable declared in a given scope in which the property/sequence is defined is available to the assertion. If the assertions are declared out of the module but bound to the module using 'bind' method, the same rule applies. More on 'bind' statement coming up soon.

In this example, the sampling edge will be the posedge of (clk && cGate). In the preponed region of this sampling edge, the variables in property and sequence will be sampled.

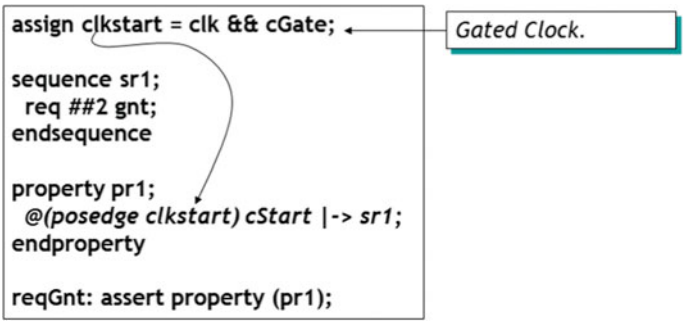


Fig. 4.12 Gated clock

4.4 Concurrent Assertions are Multi-Threaded

This is about the most important concept you need to grasp when it comes to concurrent assertions. We all know SystemVerilog is a concurrent language but is it multi-threaded (except when auto variables are used)? SVA is by default concurrent and multi-threaded.

```
sequence sr1;
  req ##2 gnt;
endsequence

property pr1;
  @(posedge clk) cStart |-> sr1;
endproperty

reqGnt: assert property (pr1)  $display($stime,,,"\t\t %m PASS");
else $display($stime,,,"\t\t %m FAIL");
```

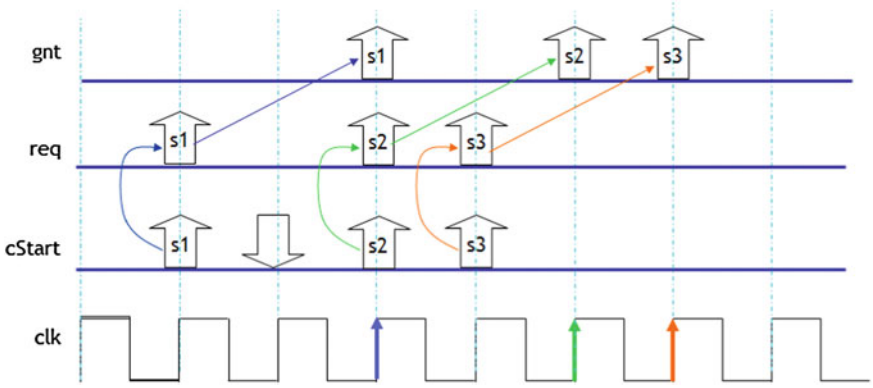


Fig. 4.13 Multi-threaded concurrent assertions

In Fig. 4.13, we have declared the same assertion that you have seen before, namely at posedge clk, if cStart is sampled high that sr1 will be triggered at the same posedge clk which will then look for 'req' to be high at that clock and 'gnt' to be sampled high two clocks later.

Now, let us say that cStart is *sampled* high (S1) at a posedge of clk and that 'req' is also sampled high at that same edge. After this posedge clk, the sequence will wait for 2 clocks to see if 'gnt' is high.

But before the two clocks are over, clk cStart goes low and then goes high (S2) exactly two clocks after it was sampled high. This is also the same edge when our first trigger of assertion will look for gnt to be high (S1). So, what will the assertion do? Will it re-fire itself because it meets its antecedent condition (S2) and ignore 'gnt' that it is been waiting for from the first trigger (S1)? No, it will not ignore 'gnt'. It will sample 'gnt' to be high (S1) and consider the first trigger (cStart (S1)) to PASS. So, what happens to the second trigger (cStart (S2))? It will start another thread. It will again wait for 2 clocks to check for 'gnt'. So far so good. We see one instance of SVA being threaded.

But life just got more interesting.

After S2, the very next clock cStart is sampled high again (S3). And 'req' is high as well (req(S3)). Now what will the assertion do? Well, S3 will thread itself with S2. In other words, there are now two distinct triggers of the same assertions waiting to sample 'gnt' two clocks after their trigger. The figure perfectly (!) lines up 'gnt' to be high two clocks after both S2 as well as after S3 and all 3 triggers of the same assertions will PASS.

This has many implications in terms of design of assertions and performance thereof. We will discuss this further when we discuss edge triggered antecedent. In other words, the way the property in our example is coded, it will drag your simulation performance because every time the property sees cStart to be high at posedge of clk, it will start a new thread. But if you want to evaluate the property only at the first rise of cStart and then ignore it if it stays high (unless it goes low and goes high again) then you have to use edge sensitive antecedent. More on this in Chap. 5. In addition, the concept of multi-threaded language gets much more interesting as you will see in Sect. 6.2.1.

4.5 Formal Arguments

One of the key features of assertions is that they can be parameterized. In other words, assertions can be designed with formal arguments to keep them generic enough for use with different actual arguments.

Figure 4.14 is self-explanatory. Notice that the formal arguments can be specified in a sequence, in a property as well as in the assert statement.

The application shows the advantage of formal arguments in reusability. Property 'noChangeSig' has 3 formal arguments, namely pclk, refSig and Sig. The property checks to see that if refSig is sampled high at posedge pclk, that the Sig is not unknown. Once such a generic property is written you can invoke it with

different clk, different refSig and Sig. CheckRd is a property that uses sysClk and OE_ and RdData to check for unknown condition while CheckWr uses WE_ and WrData to check for WrData to be not unknown.

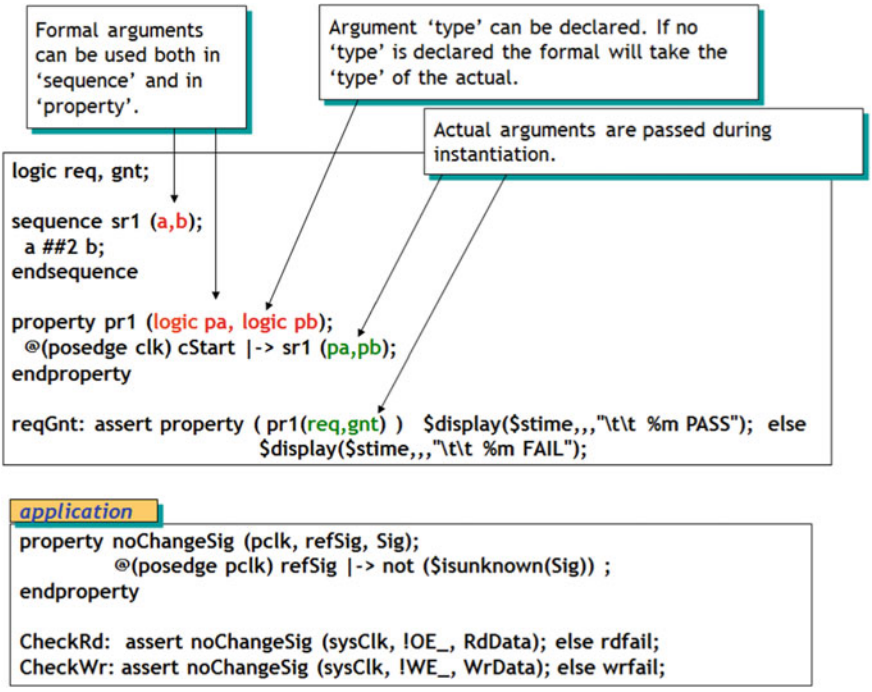


Fig. 4.14 Formal and actual arguments

In any project, there are generic properties that can be reused multiple times by passing different actual arguments. This is reusable not only in the same project but also among projects.

Companies have created libraries of such pool of properties that projects look up and reuse according to their needs.

As shown in Fig. 4.15, properties can be both position based as well as name based. I highly recommend name based to make sure that actuals are connected to correct formals without ambiguity. This rule is the same as that we have been using for Verilog port connections.

Figure 4.16 describes the following points

(1) Default values can be assigned to the formal arguments.

   a. If actual and formal both specify a 'default' value, the actual will overwrite the formal default value
   b. You may leave passing an actual to a formal if the formal has a default value. Please refer to Fig. 4.16.

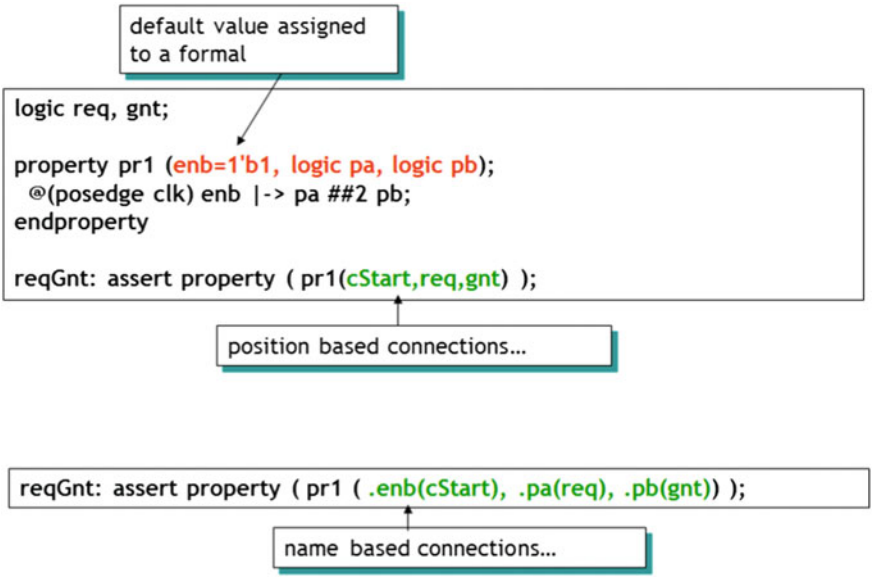


Fig. 4.15 Formal and actual arguments—default value and name based connection

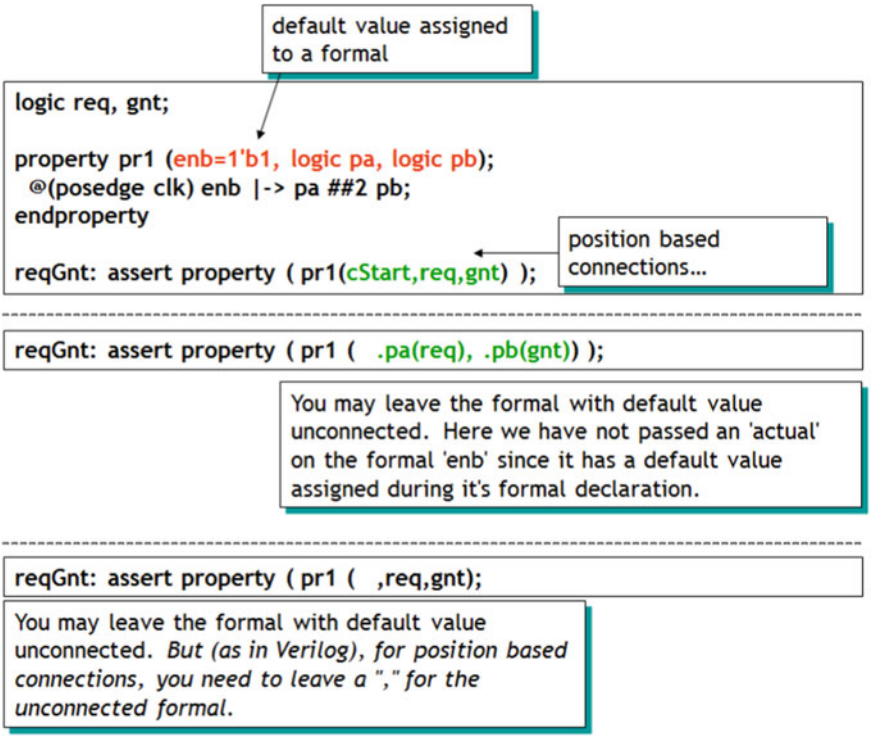


Fig. 4.16 Formal and actual arguments—default value and position based connection

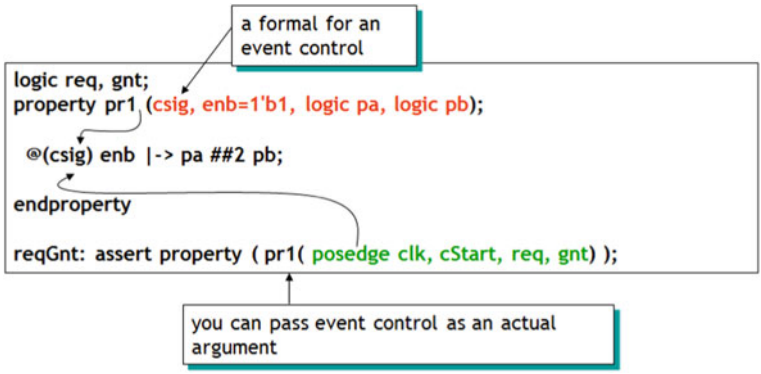


Fig. 4.17 Passing event control to a formal

This is a very interesting feature and very useful at that for reusability. A formal can be used for event control as well. A sampling edge can be passed as an actual to a formal and the actual can be used as a sampling edge in the property. We are passing 'posedge clk' as an actual to the formal 'csig'. The property uses @ (csig) as it is sampling edge. '@ (csig)' will change to '@ (posedge clk)' when the property 'pr1' is called with 'posedge clk' as the actual argument. Please refer to Fig. 4.17 for clarity on this point. Such properties can indeed be part of a common pool of properties that individual projects can reuse with their own sampling edge specification.

4.6 Disable (Property) Operator: 'disable iff'

Of course, you need a way to disable a property under conditions when the circuit is not stable (think Reset). That is exactly what 'disable iff' operator does. It allows you to explicitly disable the property under a given condition. Note that 'disable iff' reads as 'disable if and only if'. The example in Fig. 4.18 shows how you can disable an assertion during an active Reset. There is a good chance you will use this Reset based disable method in all your properties throughout the project. Note below the rules governing 'disable iff'

(1) 'disable iff' can be used only in a property—not a sequence.
(2) 'disable iff' can only be used before the declaration of the antecedent condition.

Ok, so what happens if a property has started executing and the 'disable iff' condition occurs in the middle of its execution?

The property in Fig. 4.18 checks to see that sdack_ falls (i.e. contained) within soe_ (donot worry, we will see how such properties work in later chapters). It also has the 'disable iff (! reset)' condition. Disable this property if reset is asserted (active low).

Let us examine the simulations logs.

Fig. 4.18 'disable iff' operator

In the LHS simulation log, reset is never asserted and the assertion completes (and passes in this case).

In the RHS simulation block, reset is asserted in the middle of check "sdack_ within soe". Guess what, the entire assertion is discarded. You will not see pass/fail for this assertion because it has been discarded. Entire assertion is disabled if the disable iff condition occurs in the middle of an executing assertion. Some folks mistake such discard as a failure, which is incorrect.

Once an assertion has been disabled with 'disable iff' construct, it will re-start only after the 'disable iff' condition is not true anymore.

As we will discuss in Sect. 7.4, there are system tasks that provide global control over execution of assertions.

4.7 Severity Levels (for Both Concurrent and Immediate Assertions)

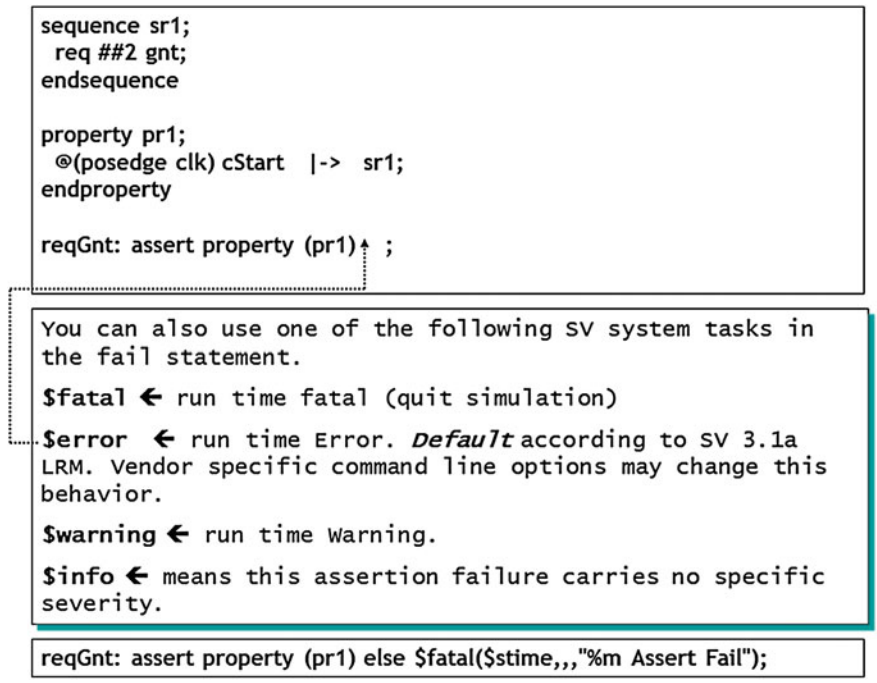


Fig. 4.19 Severity levels for concurrent and immediate assertions

Assertions also allow error reporting with different severity levels. $fatal, $error (default), $warning and $info. Figure 4.19 explains meaning of each.

$error is default, meaning if no failure clause is specified in the assert statement, $error will kick in and provide a simulator generated error message. If you have specified a label (and you should have) to the assertion, that will be (most likely) displayed in the $error message. I say most likely because the SystemVerilog LRM does not specify exact format of $error. It is simulator vendor specific. $warning and $info are self-explanatory as described in the Fig. 4.19.

4.8 Binding Properties

'bind' allow us to keep design logic separate from the assertion logic. Design managers do not like to see anything in RTL that is not going to be synthesized. 'bind' helps in that direction.

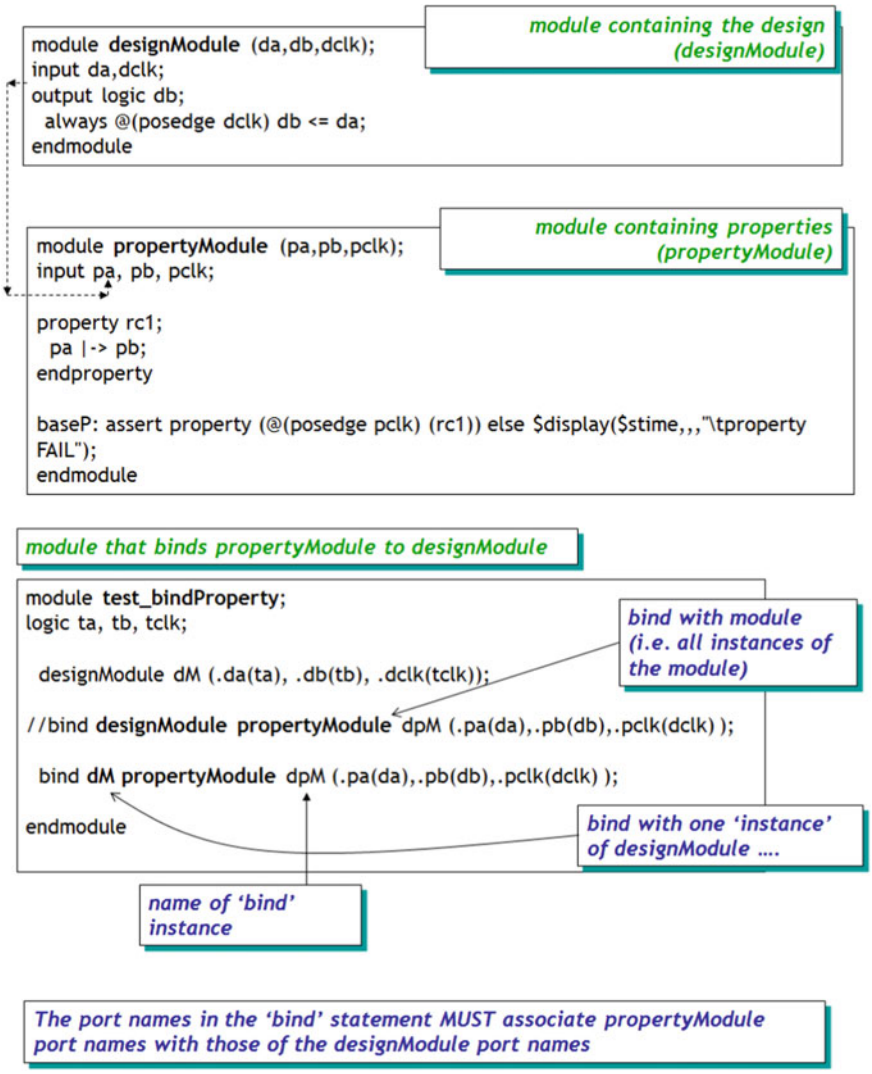


Fig. 4.20 Binding properties

There are three modules in Fig. 4.20. The 'designModule' contains the design. The 'propertyModule' contains the assertions/properties that operate on the logic in 'designModule'. And the 'test_bindProperty' module binds the propertyModule to the designModule. By doing so, we have kept the properties of the 'propertyModule' separate from the 'designModule'. That is the idea behind 'bind'. You do not have to place properties in the same module as the design module. As mentioned before, you should keep your design void of all constructs that are non-

synthesizable. In addition, keeping assertions and design in separate modules allow both the design and the DV engineers work in parallel without restrictions of a database management system where a file cannot be modified by two engineers at the same time.

In order for 'bind' to work, you have to declare either the instance name or the module name of the designModule in the 'bind' statement. You need the design module/instance name, property module name and the 'bind' instance name for 'bind' to work. In our case the design module name is designModule, its instance name is 'dM' and the property module name is propertyModule.

The (uncommented) 'bind' statement uses the module instance 'dM' and binds it to the property module 'propertyModule' and gives this 'bind' an instance name 'dpM'. It connects the ports of propertyModule with those of the designModule. With this the 'property rc1' in propertyModule will act on designModule ports as connected.

The commented 'bind' statement uses the module name 'designModule' to bind to the 'propertyModule' whereby all instanced of the 'designModule' will be bound to the 'propertyModule'.

In essence, we have kept the properties/assertions of the design and the logic of the design separate. This is the recommended methodology. You could achieve the same results by putting properties in the same module as the design module but that is highly non-modular and intrusive methodology. In addition, as noted above, keeping them separate allows both the DV and the Design engineer to work in parallel.

4.8.1 Binding Properties (Scope Visibility)

But what if you want to bind the assertions of the propertyModule to internal signals of the designModule? That is quite doable.

As shown in Fig. 4.21, 'rda' and 'rdb' are signals internal to designModule. These are the signals that you want to use in your assertions in the 'propertyModule'. Hence, you need to make 'rda' and 'rdb' visible to the 'propertyModule'. However, you do not want to bring 'designModule' internal variables to external ports in order to make them visible to the 'propertyModule'. You want to keep the 'designModule' completely untouched. To do that, you need to add input ports to the 'propertyModule' and bind those to the internal signals of the 'designModule' as shown in Fig. 4.21. Note that in our example we bind the propertyModule ports 'pa' and 'pb' to the designModule internal registers 'rda' and 'rdb'. In other words, you can directly refer to the internal signals of designModule during 'bind'. 'bind' has complete scope visibility into the bound module 'designModule'. Note that with this method you do not have to provide the entire hierarchical instance name when binding to 'propertyModule' input ports.

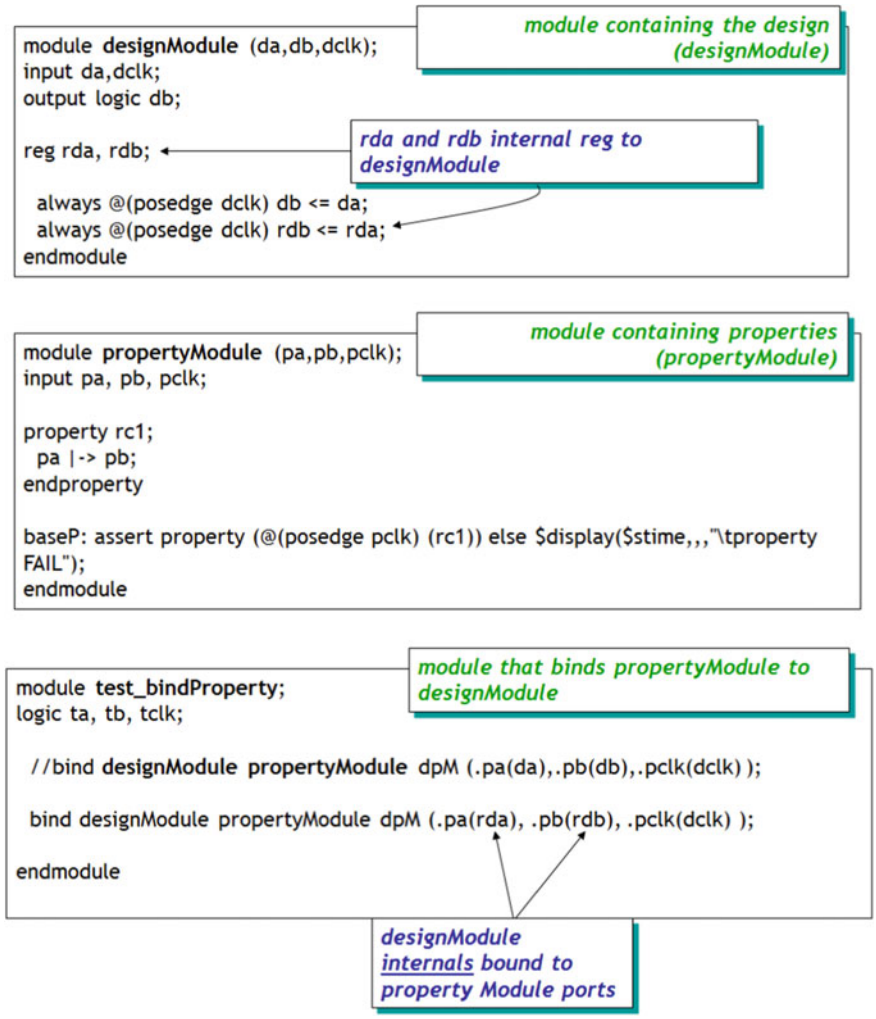


Fig. 4.21 Binding properties to design 'module' internal signals (scope visibility)

4.8.2 Assertion Adoption in Existing Design

Figure 4.22 shows that if you have an existing design, you can effectively use the 'bind' construct to write assertions outside of the design scope and bind them. This can be very useful, if you are bringing in legacy blocks in your new SoC and want to make sure that the legacy blocks work well in your new design. This figure is a methodology component. Upfront in your project, determine your 'bind' methodology. See that all the assertions are outside RTL and not a messy mix of some in RTL and some bound with external properties file.

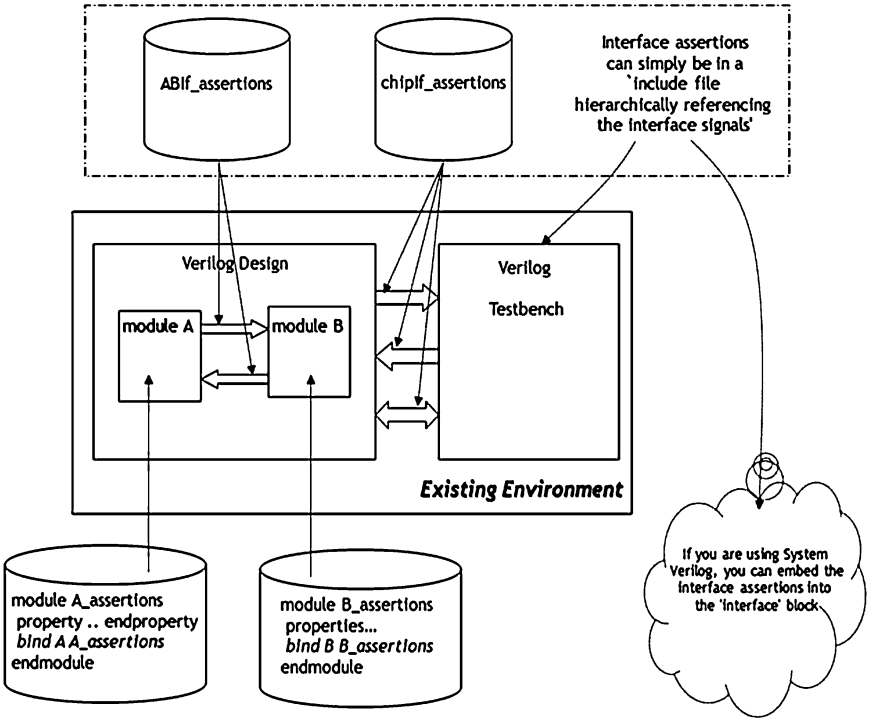


Fig. 4.22 Binding properties to an existing design. Assertions adoption in existing design

Other advantage of keeping assertions in a separate file is that they can be independently verified without the need to have control of RTL files. A big advantage when you want to make sure that both the design and verification progress in parallel.

4.9 Difference Between 'sequence' and 'property'

Now that we have seen assertions using sequences and properties, it is good to recap and clearly understand the differences between the two.

- **'sequence'**
  - A sequence is a building block. Think of it as a macro or a subroutine where you can define a specific relationship for a given set of signals.
  - A sequence on its own does not trigger. It must be asserted.
  - A sequence does not allow implication operator. Simply allows temporal (or combinatorial) domain relationship between signals.

- A sequence can have optional formal arguments.
- A clocking event can be used in a sequence.
- A sequence can be declared in a module, an interface, a program, a clocking block, a package (***but –not- in a*** '***class***').

- **'property'**
  - A property also does not trigger by itself until 'assert'ed (or 'cover'ed).
  - Properties have implication operator that imply the relationship between an antecedent and a consequent.
  - Sequences can be used as building blocks of complex properties.
  - Clocking event can be applied in a property, in a sequence, or in both.
  - A property can be declared in a module, an interface, a program, a clocking block, a package (***but –not- in a*** '***class***').

Chapter 5
Sampled Value Functions $rose, $fell

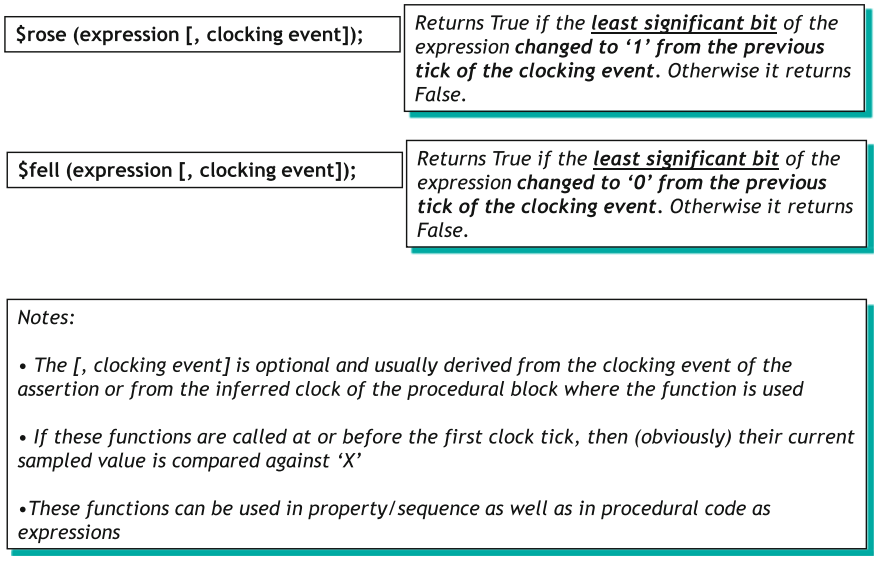


Fig. 5.1 Sampled value functions $rose, $fell—basics

These sampled value functions allow for antecedent and/or the consequent to be edge triggered. $rose means that the expression (in $rose(expression)) was sampled to be '0' (or 'x' or 'z') at the previous clk edge (previous meaning the immediately preceding clk from current clk) and that it is sampled '1' at this clk edge. For $fell, just the opposite need to take place. Preceding value should be sampled '1' (or 'x' or 'z') and current value '0'. As explained with examples below, one needs to understand the difference between level sensitive sample versus edge sensitive sample (Fig. 5.1).

But why do we call these functions 'sampled value'? That's because they are triggered only when the sampled value of the expression in the preponed region

A. B. Mehta, *SystemVerilog Assertions and Functional Coverage*,
DOI: 10.1007/978-1-4614-7324-4_5,

differ at two successive clock edges as described above. In other words, $rose(abc) does *not* mean 'posedge abc' as in Verilog. $rose(abc) does not evaluate to true as soon as abc goes from 0 to 1. $rose(abc) simply means that abc was sampled '1' at the current clock edge (in preponed region) and that it was not sampled a '1' at the immediately preceding clock edge (in the preponed region).

Note also that both $rose and $fell work only on the Least Significant Bit of the expression. You will soon see what happens if you use a bus (vector) in these two sampled value functions.

5.1 $rose: Edge Detection in Property/Sequence

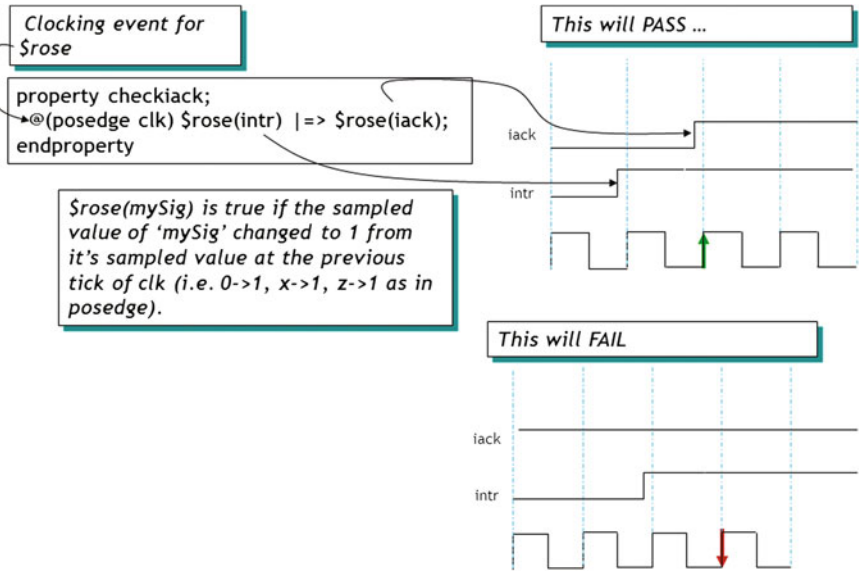


Fig. 5.2 $rose—basics

Property 'checkiack' in the top logic/timing diagram will (Fig. 5.2) PASS because both the 'inter' and 'iack' signals meet the required behavior of $rose (value at two successive clks are different and are '0' followed by '1'). However, the logic in the bottom diagram fails because while $rose(intr) meets the requirement of $rose, 'iack' does not. 'iack' does not change from '0' to '1' between the two clk edges.

Important Note: To reiterate the points made above. $rose does *not* mean posedge and $fell does *not* mean negedge. In other words, the assertion won't consider $rose(intr) to be true as soon as a posedge on 'intr' is detected. The $rose()/$fell() behavior is derived by 'sampling' the expression at two successive clk edges and see if the values are opposite and in compliance with $rose() or $fell().

In other words, the fundamental of concurrent assertions specifies that everything must be sampled at the sampling edge. Behavior is based on sampled value.

5.1.1 Edge Detection is Useful Because …

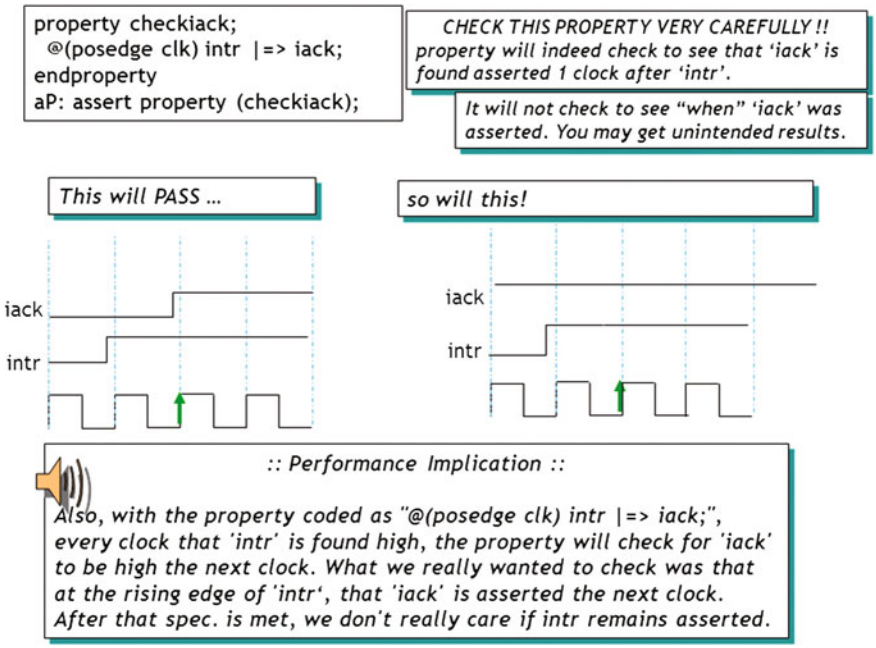


Fig. 5.3 Usefulness of 'edge' detection and performance implication

This is a very important example. It explains the difference between use of level sensitive sampled values versus edge sensitive. Both are correct to use, except that you need to know which to use when. As shown in Fig. 5.3, level sensitive evaluation is a superset of edge sensitive evaluation. But when you use level sensitive sample, you will degrade simulation performance, if in fact you meant for an edge sensitive evaluation.

In the above property, the following would be more appropriate if all you wanted to do was to check for iack to go from inactive ('0') state to active state '1' once edge-sensitive intr is asserted. After that, the state of intr does not matter. Following is a better way to write the property if your intention was to check for rigging edge of iack one clock after rising edge of intr.

property checkiack;
@ (posedge clk) $**rose**(intr) |=> $**rose**(iack);
endproperty

But what if you decide to do the following (as shown in Fig. 5.4)? Now you are courting real trouble. As Fig. 5.4 explains, since 'intr' is level sensitive sample, when it is sampled high it will look for the edge sensitive 'iack'. BUT since 'intr' is level sensitive and high the very next clock, it will start a new thread and check for $rose(iack) every clock. Since iack did not go from '0' to '1'on this second thread, the property fail. There is very good chance you did not want to see this failure.

```
property checkiack;
  @(posedge clk) intr  |=>
$rose(iack);
endproperty
aP: assert property  (checkiack);
```

So, you decide to use $rose(iack) to make sure that iack indeed was low before it was detected to be high.

But.... intr is still level sensitive...

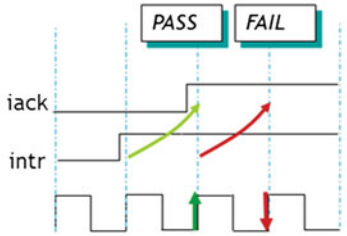


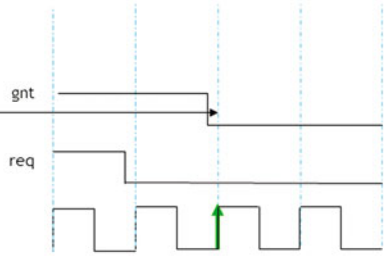
Fig. 5.4 $rose—finer points

In short, as simple as these functions look, you have to be careful in their usage and also keep in mind performance implications (Fig. 5.5).

5.1.2 $fell: Edge Detection in Property/Sequence

Clocking event for $fell

```
sequence sfell(a);
  $fell(a);
endsequence
property srose;
  @(posedge clk) $fell(req)  |=>
sfell(gnt);
endproperty
```



$fell(a) is true if the sampled value of 'a' changed to 0 from it's sampled value at the previous tick of clk (i.e. 1->0, x->0, z->0 as in negedge).

application

```
property checkWrData;
  @(posedge clk) ($fell(we_))  |-> not ($isunknown(wData)) ;
endproperty
```

Fig. 5.5 $fell—basics

5.1.3 $rose, $fell: In Procedural

$rose and $fell are very useful not only in concurrent assertions but also in sequential procedural block. They work exactly the same way as in concurrent assertions. Please see the examples in Fig. 5.6.

Since every assertion requires a clocking event (i.e. sampling edge), when you use a concurrent assertion in a procedural code without an explicit clocking event associated with them, the simulator looks for a clocking event in the code that precedes the concurrent assertion. We will discuss more on use of concurrent assertions in procedural code, under the Advanced Topics section.

In Fig. 5.6, $(posedge clk) is the preceding clocking event and acts as the sampling edge for $rose (iStreamDone) (example at the top of the figure).

Note the use of $rose and $fell in continuous assignment statement. Since continuous assign cannot have an edge behavior, you have to explicitly embed a clocking event with $rose() and/or $fell(). This is the same rule that applies to other sampled value functions.

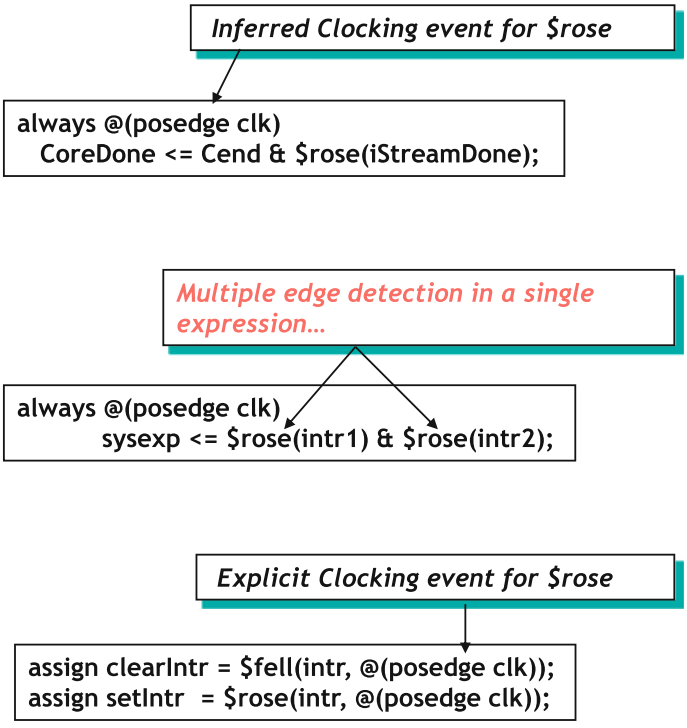


Fig. 5.6 $rose and $fell in procedural block and continuous assignment

5.2 $stable

$stable(), as the name implies, looks for its expression to be stable between two clock edges (i.e. two sampling edges). It evaluates the expression at current clock edge and compares it with the value sampled at the immediately preceding clock edge. If both values are same, the check passes (Fig. 5.7).

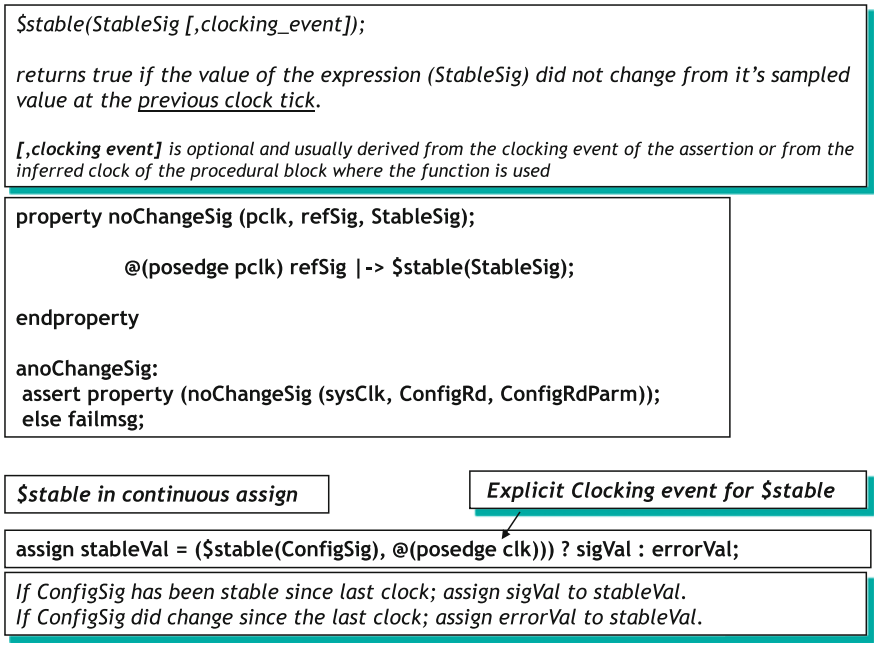


Fig. 5.7 $stable—basics

Note the use of $stable in continuous assignment statement. Since continuous assign cannot have an edge behavior, you have to explicitly embed a clocking event with $stable. This is the same rule that applies to other sampled value functions.

But what if you want to check if the signal has been stable for more than 1 clock? Read on… $past() will solve that problem.

5.2.1 $stable in Procedural Block

As in $rose() and $fell(), $stable can also be embedded in the procedural code and works the same way as in a property or a sequence. As shown in the example above, $stable samples the value of expression (‘a’ and ‘b’ in this example) at the

current and the immediately preceding edge (posedge clk in this example) to see if the value of the expression did not change. At time 15, 'b' has been stable, at time 25 'a' has been stable and so on (Fig. 5.8).

```
always @(posedge clk)
begin
  if ($stable(a)) $display ($stime,,,"\t 'a' stable from previous clock");
  if ($stable(b)) $display ($stime,,,"\t 'b' stable from previous clock");

  if ($stable(a) && $stable(b))
    $display ($stime,,,"\t 'a' AND 'b' Stable this clock");
end
```

```
# run -all
#        5  clk=1 a=1 b=0
#       15  clk=1 a=0 b=0
#       15    'b' stable from previous clock

#       25  clk=1 a=0 b=1
#       25    'a' stable from previous clock

#       35  clk=1 a=1 b=0
#       45  clk=1 a=1 b=1
#       45    'a' stable from previous clock

#       55  clk=1 a=1 b=1
#       55    'a' stable from previous clock
#       55    'b' stable from previous clock
#       55    'a' AND 'b' Stable this clock
```

Fig. 5.8 $stable in procedural block

5.3 $past

$past() is an interesting function. It allows you to go in past as many clocks as you wish to. You can check for an 'expression 1' to have a certain value, number of clocks (strictly prior time ticks) in the past. Note that number of ticks is optional. If you do not specify it, the default will be to look for 'expression 1' one clock in the past.

Another caveat that you need to be aware of is when you call $past in the initial time ticks of simulation and there are not enough clocks to go in the 'past'. For example, you specify "a |-> $past (b)" and the antecedent 'a' is true at time '0'. There isn't a clock tick to go in the past. In that case, the assertion will use the 'initial' value of 'b'. What is the initial value of 'b'? It's not the one in the 'initial' block, it's the value with which the variable 'b' was declared (as in "logic b = 1'b1;"). In our case, if 'b' was not initialized in its declaration, the assertion will fail. If it was declared with an initial value of 1'b1, the assertion will pass.

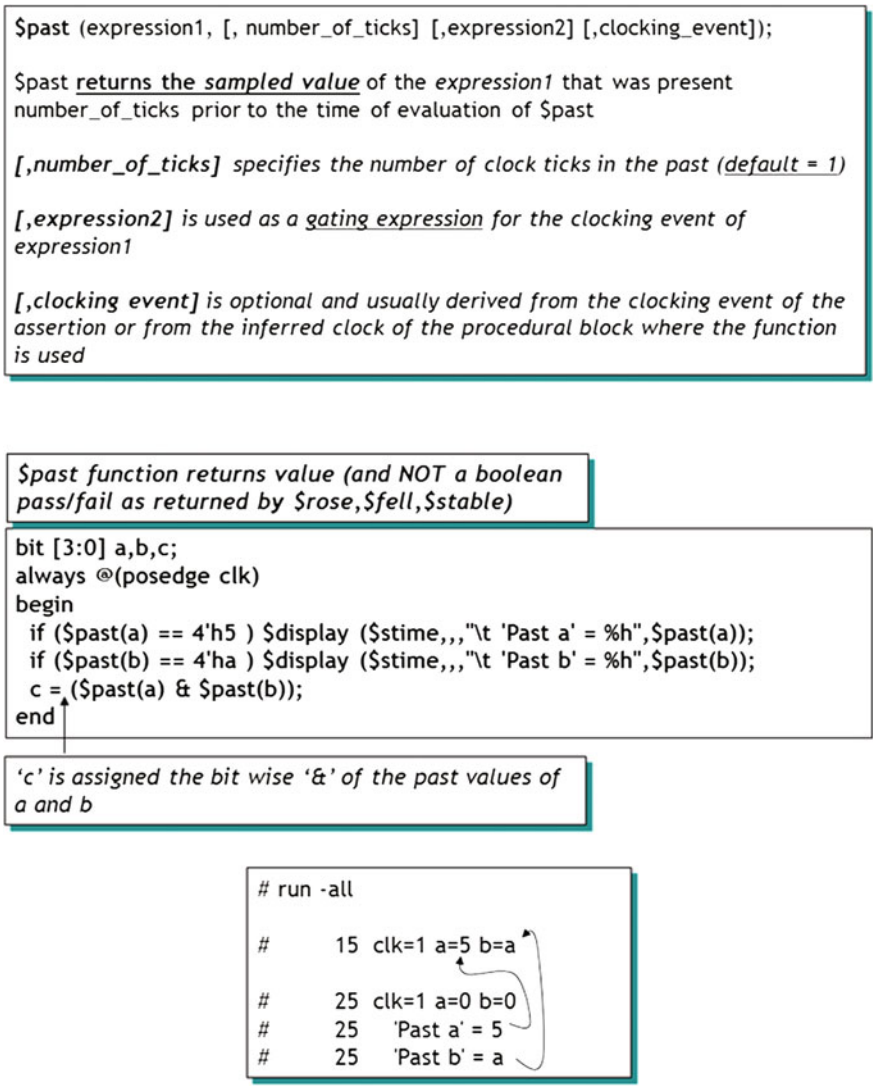


Fig. 5.9 $past—basics

You can also 'gate' this check with expression 2. The example in Fig. 5.9 shows how $past works. We are using a gating expression in this example. It is not a requirement as noted in the Fig. 5.10, but it will most likely be required in your application. If expression 2 is not specified, no clock gating is assumed.

If you understand the use of $past with a gating expression, then its use without one will be straightforward to understand.

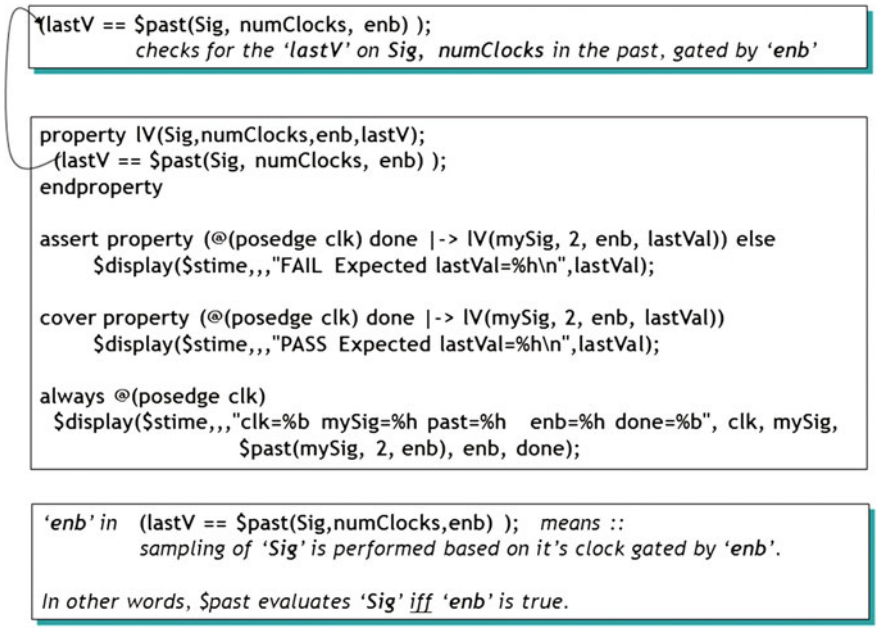


Fig. 5.10 $past—gating expression

Figure 5.10 asserts the following property

assert property (@ posedge clk) done |-> lV(mySig,2,enb,lastVal) $display(….);

And the property lV models the following

property lV(Sig, numClocks, enb, lastV);
(lastV == $**past**(Sig, numClocks, enb));
endproperty

The property says check on Sig, numClocks in the past and see if it has the value 'lastV' and do this check if and only if 'enb' (the gating expression) is high when you *start* the check (i.e. when antecedent done = 1 in the assert statement). *Let me re-emphasize that the gating expression is checked when the 'antecedent' is true*. When you *start* the check, the gating expression need to be true. Many seem to miss this point. Let us look at the simulation log which will explain this concept. The example from previous page is repeated here with lastV = 'ha when we assert/cover the property 'lV' (stands for Last Value) for easy reference to the simulation log (Fig. 5.11).

Let us examine the simulation log carefully to see how $past works. At time 30, done = 1 for the first time which means that the antecedent of the property is true implying that the property lV be executed. lV has formal arguments which are replaced by the actual arguments from the assert statement.

```
property lV(Sig, numClocks, enb, lastV);
  (lastV == $past(Sig, numClocks, enb) );
endproperty

assert property (@(posedge clk) done |-> lV(mySig, 2, enb, 'ha)) else
      $display($stime,,,"FAIL  Expected lastVal=%h\n",lastVal);

cover property (@(posedge clk) done |-> lV(mySig, 2, enb, 'ha))
      $display($stime,,,"PASS  Expected lastVal=%h\n",lastVal);

always @(posedge clk)
  $display($stime,,,"clk=%b  mySig=%h past=%h   enb=%h done=%b", clk, mySig,

$past(mySig, 2, enb), enb, done);
```

```
# run -all
#       10  clk=1 mySig=a past=0  enb=1 done=0
#       20  clk=1 mySig=5 past=0  enb=1 done=0
#       30  clk=1 mySig=5 past=a  enb=1 done=1
#       30  PASS Expected lastVal=a
#
#       40  clk=1 mySig=5 past=5  enb=1 done=0
#       50  clk=1 mySig=a past=5  enb=1 done=1
#       50  FAIL Expected lastVal=a
#
#       60  clk=1 mySig=a past=5  enb=1 done=0
#       70  clk=1 mySig=5 past=5  enb=0 done=0
#       80  clk=1 mySig=5 past=5  enb=0 done=1
#       80  FAIL Expected lastVal=a
#
```

A time 80 :

Even though mySig's $past(2) value (at time 60) is "a", && enb=1, the property fails at 80 when evaluated (with done=1) because enb=0 at the current clock tick and the lastV retains the previously sampled value of "5" and the comparison with "a" fails.

Fig. 5.11 $past—gating expression—simulation log

So, at time 30, the property first checks to see if the gating signal ('enb') is true. Since it is indeed true, the property now evaluates the value of mySig 2 clocks in the past. It sees that it is indeed h' a (at time 10 in the simulation log). The property passes.

At time 50, done = 1 and enb = 1 but 2 clocks in the past (at time 30), mySig was not equal to h' a and the property fails.

At time 80, done = 1, but the gating signal 'enb' is a '0'. The interesting thing to note here is that the property fails even though the value of mySig is indeed h' a

two clocks in the past at time 60. That's because the gating expression enb = 0 at the current clock tick (when antecedent 'done' is true) and the $past() does not evaluate itself. In other words, $past() did not look for mySig 2 clocks in the past, instead returned its previously evaluated value h' 5. The property compares this value of h' 5 with expected value of h' a and fails.

Without a gating signal, the property will always evaluate whenever the antecedent is true and look for the required expression value N number of clocks in the past.

Note also the use of $past in the $display statement which is a procedural statement. This is an excellent debug feature. You can always display what happens in the past to debug the current state of design.

5.3.1 Application: $past()

application

Specification:

If current 'state' is cacheRead, the past state cannot be cacheInv (you can never Read from an invalid line)

```
property RdCacheInv;

        @(posedge clk) (state == cacheRead) |-> ($past(state) != cacheInv);

endproperty
```

application

Specification:

If pipe stall is asserted and data was ready to be sent the last clock that the current state must be data hold.

```
property dHoldCheck;

        @(posedge clk)  (  (pipeStall)
                           &&
                           ($past(State)==dataSend)
                        )
                           |->
                           (State == dataHold);

endproperty
```

Fig. 5.12 $past application

Figure 5.12 is self-explaining. Note that $past is used in consequent in the application at the top of the figure and used as an antecedent in the bottom application.

5.3.2 *$past rescues $fell!*

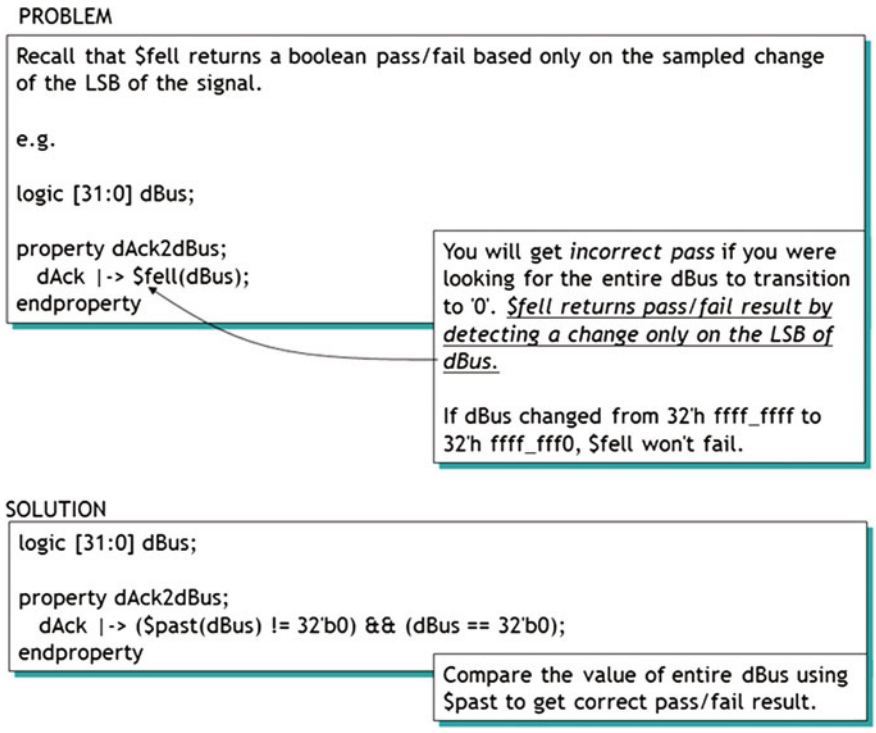


Fig. 5.13 $past rescues $fell

Figure 5.13 shows the difference between $rose/$fell with $past. Recall that $fell (or $rose) samples only the LSB of the expression/signal whose value we are evaluating. In contrast, $past evaluates the entire expression. Hence, if you want to check (for example) the value of an entire 'bus', you have to use $past. As shown in the figure, $fell will give an incorrect evaluation of the 32 bit bus 'dBus' if in fact you want to check how the entire bus evaluated at some number of clocks in the past. The figure explains how you can use $past to solve this problem which $fell could not.

Chapter 6
Operators

Following lists all the operators offered by the language (IEEE-1800, 2005). We will discuss features of 1800-2009 LRM in a separate chapter. We will examine each operator in detail since these operators are the stronghold of the language (Tables 6.1 and 6.2).

Table 6.1 Concurrent assertion operators

Operator	Description
##m **##[m:n]**	Clock delay
[*m] **[*m:n]**	Repetition—consecutive
[=m] **[=m:n]**	Repetition—non consecutive
[->m] **[->m:n]**	GoTo repetition—non consecutive
sig1 throughout seq1	Signal sig1 must be true throughout the sequence seq1
seq1 within seq2	Sequence seq1 must be contained within sequence s2
seq1 intersect seq2	'intersect' of two sequences; same as 'and' but both sequences must also 'end' at the same time
seq1 and seq2	'and' of two sequences. Both sequences must start at the same time but may end at different times
seq1 or seq2	'or' of two sequences. It succeeds if either sequence succeeds
first_match complex_seq1	Matches only the first of possibly multiple matches

A. B. Mehta, *SystemVerilog Assertions and Functional Coverage*,
DOI: 10.1007/978-1-4614-7324-4_6,

Table 6.2 Concurrent assertions operators—contd

Operator	Description
not <property_expr>	If <property_expr> evaluates to true, then not <property_expr> evaluates to false; and vice versa.
if (expression) property_expr1 else property_expr2	If…else within a property
|->	Overlapping implication operator
|=>	Non-overlapping implication operator

6.1 ##m: Clock Delay

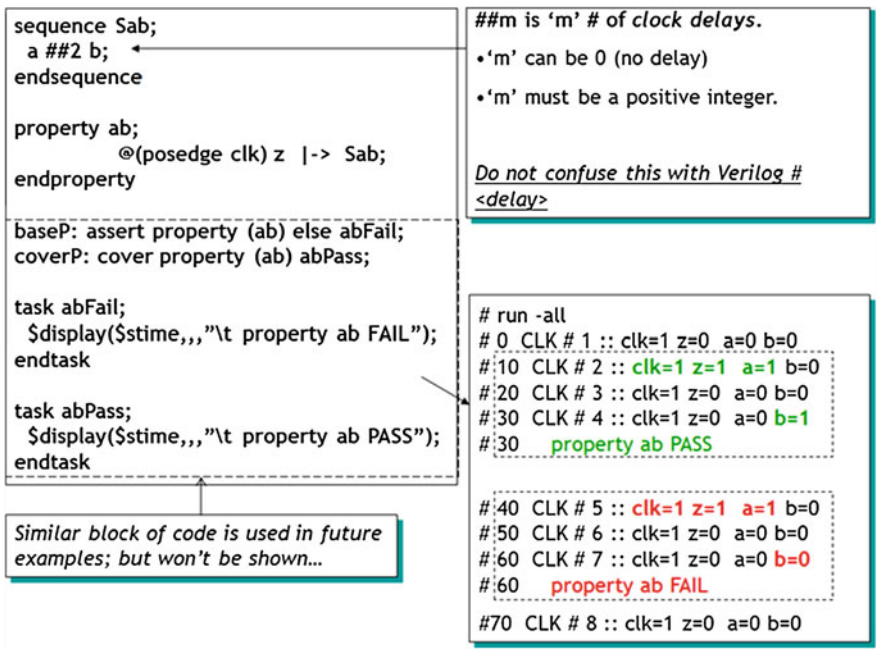


Fig. 6.1 ##m Clock delay—basics

Clock delay is about the most basic of all the operators and probably the one you will use the most! First of all, note that ##m means a delay of 'm' number of sampling edges. In this example, the sampling edge is a 'posedge clk', hence ##m means m number of posedge clks (Fig. 6.1).

The property evaluates antecedent 'z' to be true at posedge clk and implies the sequence 'Sab'. 'Sab' looks for 'a' to be true at that same clock edge (because of the overlapping operator used in the property) and if that is true, waits for two posedge clks and then looks for 'b' to be true.

In the simulation log, we see that at time 10, posedge of clk, z=1 and a=1. Hence, the sequence evaluation continues. Two clks later (at time 30), it checks to see if b=1, which it finds to be true and the property passes.

Similar scenario unfolds starting time 40. But this time, b is not equal to 1 at time 60 (two clks after time 40) and the property fails.

We can see that ##m is absolute delay. Can you have 'm' to be a variable? Short answer is No. But I have an interesting way to make it variable using a 'counter' technique. Please see section 14.8 on **"Clock Delay: What if you want** *variable* **clock delay?"**

Now, let us look at what happens if m=0. That would mean ##m is equal to ##0… hmmm, no delay!

6.1.1 Clock Delay Operator :: ##m Where m=0

```
sequence Sab;
 a ##0 b;
endsequence

property ab;
          @(posedge clk) z  |-> Sab;
endproperty
```

##0 acts as overlapping delay.

In this example, 'a' and 'b' must be '1' at the same edge of clk.

```
# run -all
#        0  CLK # 1 :: clk=1 z=0  a=0 b=0
#       10  CLK # 2 :: clk=1 z=1  a=1 b=1
#       10    property ab PASS

#       20  CLK # 3 :: clk=1 z=0  a=0 b=0
#       30  CLK # 4 :: clk=1 z=1  a=1 b=0
#       30    property ab FAIL

#       40  CLK # 5 :: clk=1 z=0  a=0 b=1
#       50  CLK # 6 :: clk=1 z=0  a=0 b=1
```

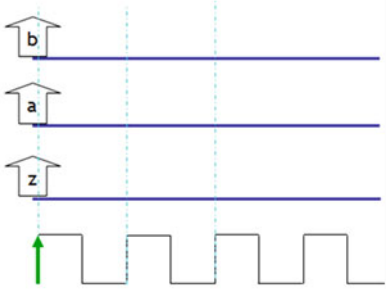


Fig. 6.2 ##m Clock delay with m=0

We examine the property as before but with m=0. As expected, the sequence 'Sab' looks for 'a' to be true and then at the same clock looks for 'b' to be true. In addition, in this property we are using overlapping implication operator, which means when 'z' is true, 'a' should be true and so should be 'b'—all at the same time. This is one of the ways you can check for multiple expressions to be true at the same sampling edge (or 'clk' edge) (Fig. 6.2).

Here is a good application where, in a complex sequence, you can effectively use ##0. Note that you could have also used '&&' in place of ##0, obviously.

6.1.1.1 Application: Clock Delay Operator :: ##m (m=0)

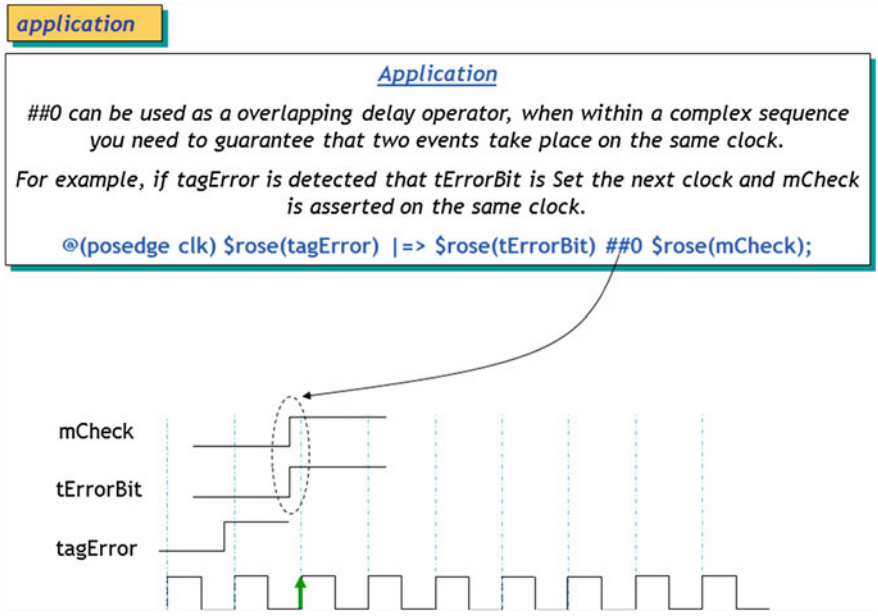


Fig. 6.3 ##0—application

See Fig. 6.3.

6.2 ##[m:n]: Clock Delay Range

Since it is quite necessary for a signal or expression to be true in a given *range* of clocks (as opposed to fix number of clocks), we need an operator that does just the same.

##[m:n] allows a range of sampling edges (clock edges) in which to check for the expression that follows it. Figure 6.4 explains the rules governing the operator. Note that here also, m and n need to be constants. They cannot be variables.

The property 'ab' in the figure says that if at the first posedge of clk that 'z' is true that sequence 'Sab' be triggered. Sequence 'Sab' evaluates 'a' to be true the same clock that 'z' is true and then looks for 'b' to be true delayed by either 1 or 2 or 3 clks. The –very- first instance that 'b' is found to be true within the 3 clocks, the property will pass. If 'b' is not asserted within 3 clks, the property will fail.

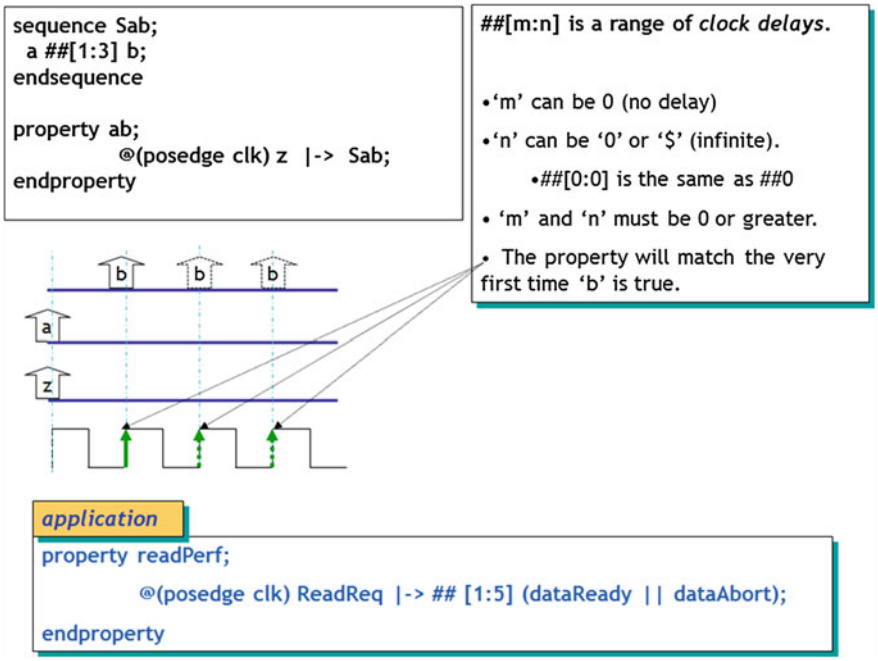


Fig. 6.4 ##[m:n] Clock delay range

Note that in the figure you see 3 passes. That simply means that whenever 'b' is true the first time within 3 clks that the property will pass. It does not mean that the property will be evaluated and pass 3 times. To reiterate, the property will pass as soon as (i.e. the first time) that 'b' is true.

6.2.1 Clock Delay Range Operator: ## [m:n] :: Multiple Threads

Back to multiple threads! But this is a very interesting behavior of multi-threaded assertions. This is something you really need to understand (Fig. 6.5).

At s1, 'rdy' is high and the antecedent is true. That implies that 'rdyAck' be true within the next 5 clks. s1 thread starts looking for 'rdyAck' to be true. The very next clock, rdyAck is not yet true but luck has it that 'rdy' is indeed true at this next clk (s2). This will fork off another thread that will also wait for 'rdyAck' to be true in the next 5 clks. The 'rdyAck' comes along within 5 clks from s1 and that thread is satisfied and will pass. But the second thread will also pass *at the same time*, because it also got its 'rdyAck' within the 5 clks that it was waiting for.

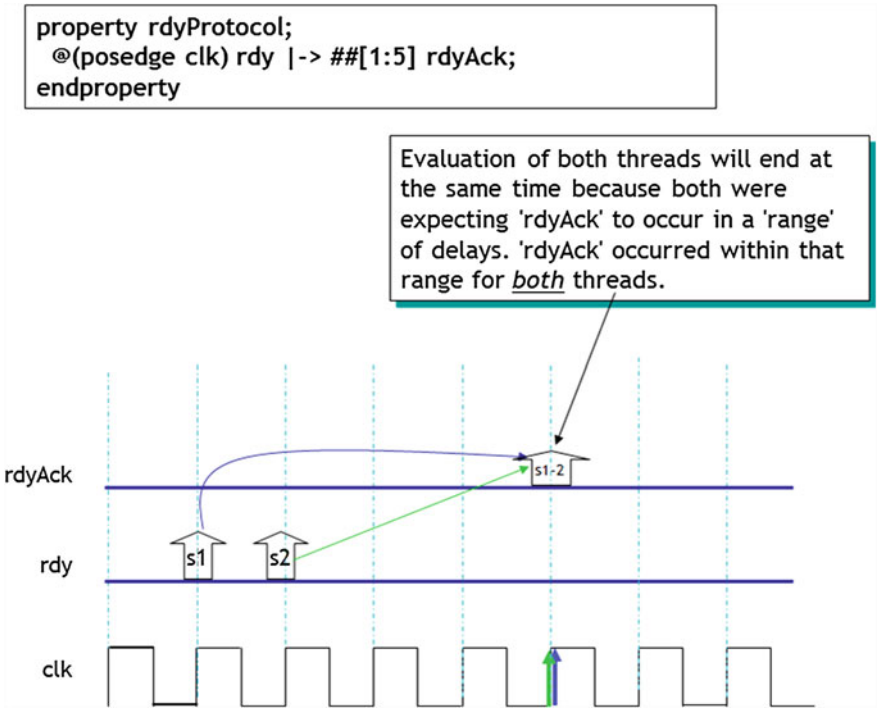


Fig. 6.5 ##[m:n]—multiple threads

This is a –very- important point to understand. *The range operator can cause multiple threads to complete at the same time.* This is in contrast to what we saw earlier with ##m constant delay where each thread will always complete only after the fixed ##m clock delays. There is a separate end to each separate thread. With the range delay operator multiple threads can end at the same time.

One hint is to keep the antecedent an edge sensitive function. For example, in the above example, instead of "@ (posedge clk) rdy" we could have used "@ (posedge clk) $rose(rdy)" which would have triggered the antecedent only once and there would not be any confusion of multiple threads ending at the same time. This is a performance hint as well. Use edge sensitive sampled value functions whenever possible. Level sensitive antecedent can fork off unintended multiple threads affecting simulation performance.

6.2.2 Clock Delay Range Operator :: ##[m:n] (m=0; n=$)

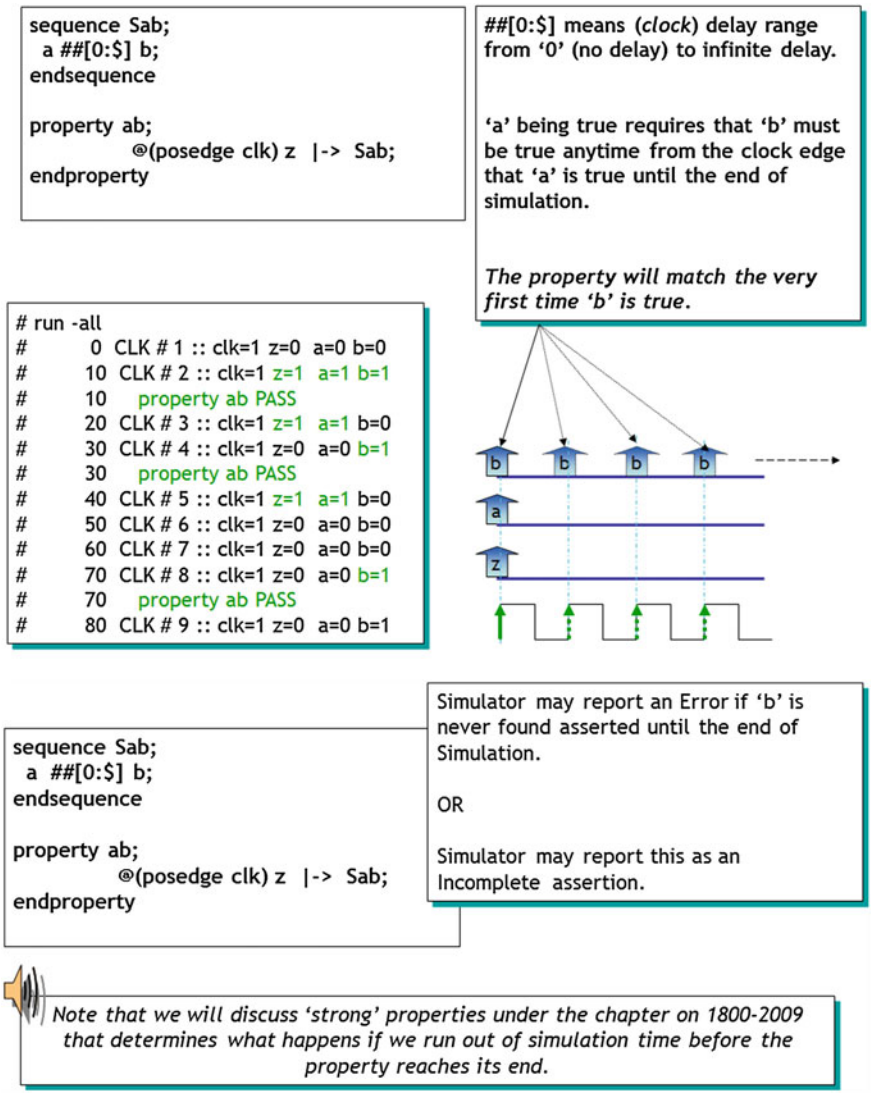


Fig. 6.6 ##[m:n] Clock delay range with m=0 and n=$

In Fig. 6.6 we are going extreme at both ends of the range, from 0 to infinity ('$' means infinite delay). As explained above, the sequence 'Sab' will look for 'b' to be true the same time as 'a' or expect it to be true any time until the simulator ends. It is fine and good if it finds 'b' to be true before simulation ends. If not, the simulator will (should) give a Warning that this assertion remains incomplete.

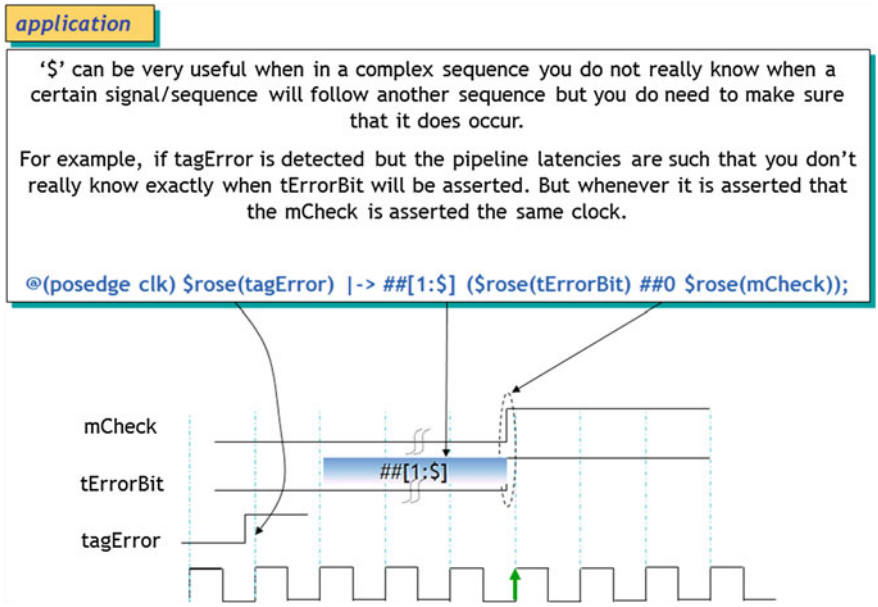


Fig. 6.7 ##[1:$] Delay range application

This example is similar to what we saw earlier. But in this example, we expect 'tErrorBit' to rise in a certain range of clock delays. The figure explains how the assertion works. Note also that you could use '&&' in place of ##0 to achieve the same results. Since assertions are mainly temporal domain, I prefer to tie in everything with temporal domain constructs. But that's a matter of preference (Fig. 6.7).

6.3 [*m]: Consecutive Repetition Operator

As depicted in Fig. 6.8 the consecutive repetition operator [*m] sees that the signal/expression associated with the operator stays true for 'm' consecutive clocks. Note that 'm' *cannot* be $ (infinite # of consecutive repetition).

The important thing to note for this operator is that it will match at the *end* of the last iterative match of the signal or expression.

The example in Fig. 6.8 shows that when 'z' is true that at the next clock, sequence 'Sc1' should start its evaluation. 'Sc1' looks for 'a' to be true and then waits for 1 clock before looking for 2 consecutive matches on 'b'. This is depicted in the simulation log. At time 10 'z' is high; at 20 'a' is high as expected (because of non-overlapping operator in property); at time 30 and 40, 'b' remains high

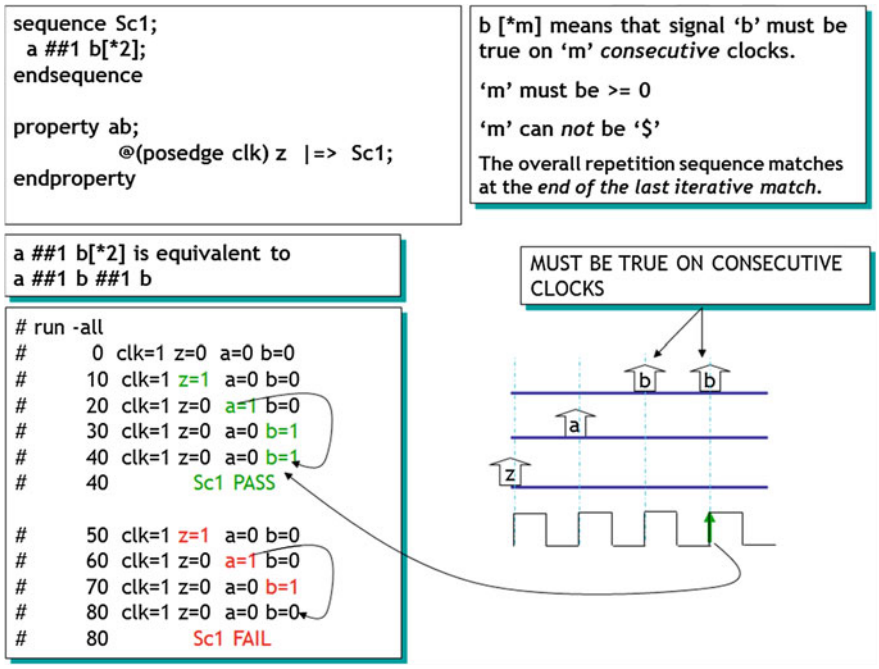


Fig. 6.8 [*m]—Consecutive repetition operator—basics

matching the requirement b[*2]. At the end of the second high on 'b' the property meets all its requirements and passes.

The very next part of the log shows that the property fails because 'b' does not remain high for two consecutive clocks. Again, the comparison ends at the *last* clock where the consecutive repetition is supposed to end and then the property fails.

Figure 6.9 shows an interesting application where we effectively use the 'not' of the repetition operator. At posedge busClk, if ADS is high that starting the same busClk (overlapping operator), ADS is checked to see if it remains high consecutively for 2 busClk(s). If it does then we take a 'not' of it to declare that the property has failed. This is a very useful property, as simple as it looks. In many protocols one needs to make sure that certain signals follow very strict protocol. This application models just such a protocol. Note also the use of parameterized property.

Interesting note is that if ADS is high for three consecutive clocks, the property will fail twice during those 3 clocks. Please see if you can figure out why. Hint, 'Sig is level sensitive'.

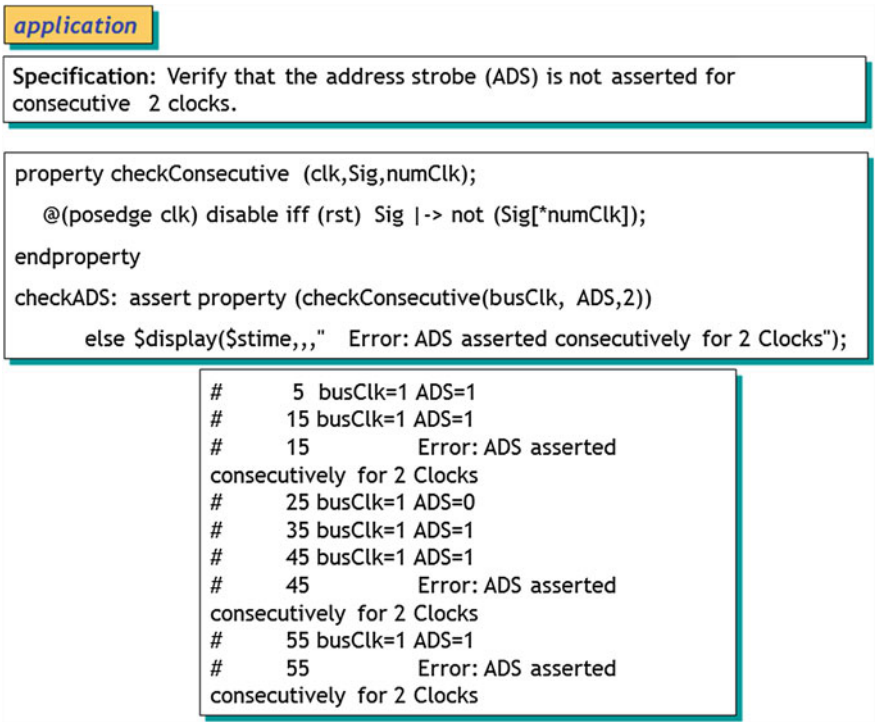


Fig. 6.9 [*m] Consecutive repetition operator—application

6.4 [*m:n]: Consecutive Repetition Range

This is another important operator that you need to understand carefully how it works, as benign as it appears to be.

Let us start with the basics. sig[*m:n] means that sig should remain true for minimum 'm' number of consecutive clocks but no more than (maximum) 'n' number of clocks. That is simple enough. But here is the first thing that differs from the sig[*m] operator we just learnt. The consecutive range operator match ends at the *first* match of the sequence that meets the required condition. Note this point carefully. It ends at the *first* match of the range operator (in contrast the non-range operator [*m] which ends at the last match of the 'm').

Figure 6.10 outlines the fact that b[*2:5] is essentially an OR of four different matches. When any one of these four sequences matches that the property is considered to match and pass. In other words, the property first waits looking for two consecutive high on 'b'. If it finds that sequence, the property ends and passes. If it does not find the second 'b' to be true, the property will fail. It does *not* wait for the third consecutive high on 'b' because there is not a third consecutive 'b' if it was not consecutively high in the second clock. The chain was already broken.

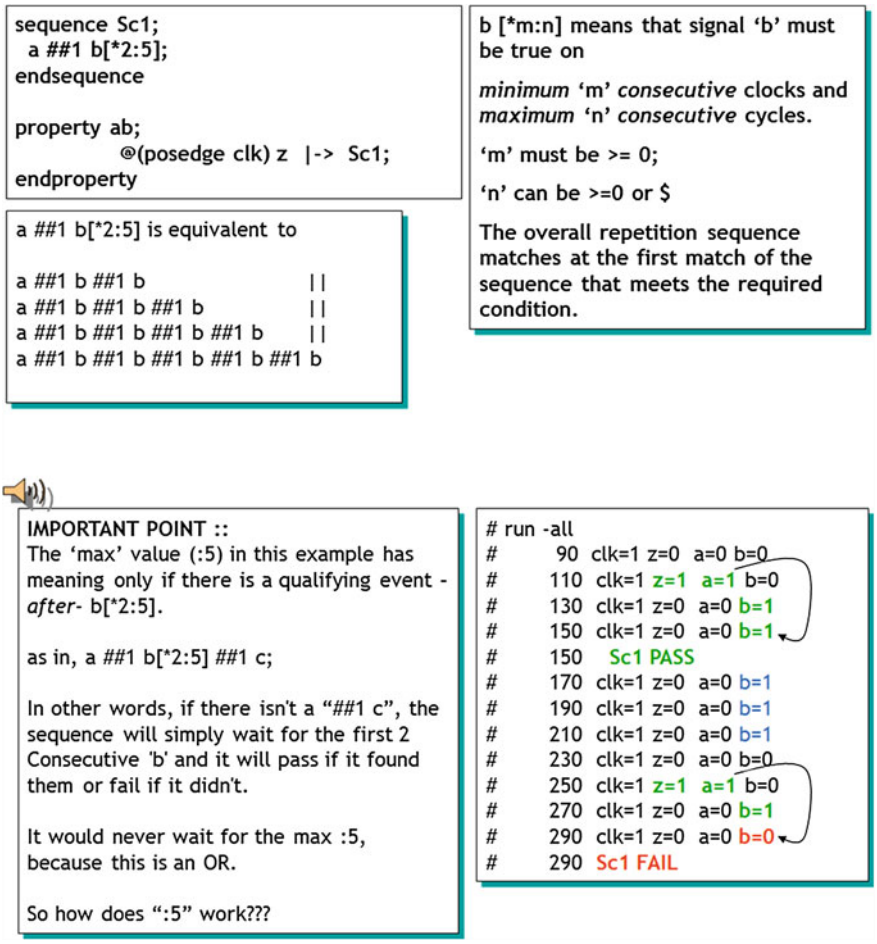


Fig. 6.10 [*m:n] Consecutive repetition range—basics

So, if 'b' arrives in the second clock, the property will pass. If 'b' was not true in the second clock, the property would fail. It will not wait for the max range.

Back to the range b[*2:5]. If you think about it, :5 will *never* get executed !! If 'b' is true for two consecutive clocks, the property matches and ends (because the property ends at first match). And if 'b' was not true for two consecutive edges, the property will fail. Please study simulation log in Fig. 6.10 carefully.

So, why do we need the max range? When does the maximum range: 5 come into picture? What does: 5 really mean? See Fig. 6.11, it will explain what max range: 5 means and how it gets used.

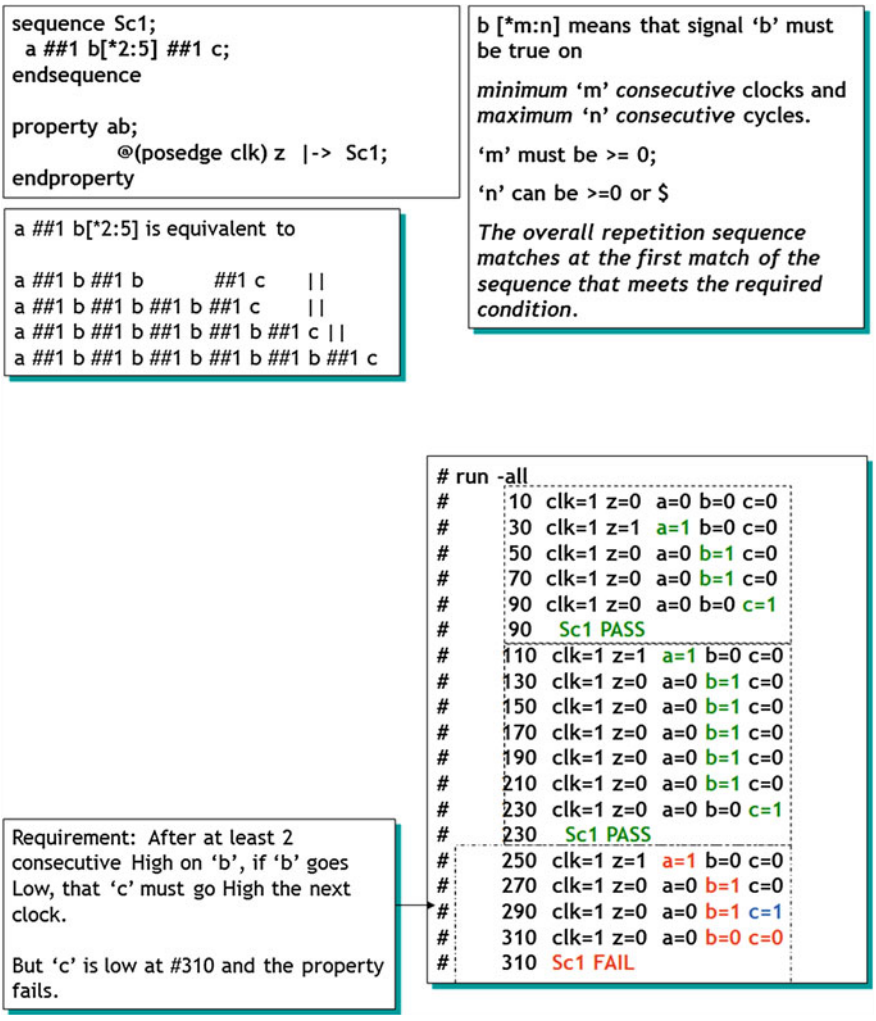


Fig. 6.11 [*m:n] Consecutive repetition range—example

Note that we added '##1 c' in sequence Sc1. It means that there must be a 'c' (high) 1 clock after the consecutive operator match is complete. Ok, simple enough.

Now let's look at the simulation log. Time 30–90 is straightforward. At time 30, z=1 and a=1, the next clock 'b'=1 and remains '1' for two consecutive clocks and then 1 clock later c=1 as required and the property passes. But what if 'c' was not equal to '1' at time 90? That is what the second set of events show.

Z=1 and a=1 at time 110 and the sequence Sc1 continues. OK. b=1 the next 2 clocks. Correct. But why doesn't the property end here? Is not it supposed to end at

the first match? Well, the reason the property does not end at 150 is because it needs to wait for c=1 the next clock. OK, so it waits for C=1 at 170. But it does not see a c=1. Should not the property now fail? NO. This is where the max range: 5 comes into picture. Since there is a range [*2:5], if the property does not see a c=1 after the first two consecutive repetition of 'b', it waits for the next consecutive 'b' (total 3 now) and then looks for 'c=1'. If it does not see c=1 it waits for the next consecutive b=1 (total 4 now) and then looks for c=1. Still no 'c'? It finally waits for max range 5th b=1 and then the next clock looks for c=1. If it finds one, the property ends and passes. If not, the property fails.

Continuing with the simulation log, the last part shows how the property would fail. One way it would fail is what I have described above. The other way is shown in the log file. I have repeated the log file here to help us concentrate only on that part of the log file.

250 clk=1 **z=1 a=1** b=0 c=0
270 clk=1 z=0 a=0 **b=1** c=0
290 clk=1 z=0 a=0 **b=1** c=1
310 clk=1 z=0 a=0 **b=0 c=0**
310 Sc1 FAIL

At time 250, z=1 and a=1 so the sequence evaluation continues to consecutive operator. 'b' is equal to 1 for the next two consecutive clocks. Good. But at time 310, b=0 *and* –also- c=0. Hence the property fails. After two consecutive 'b', there should be either a third 'b' or a 'c=1'. Neither of them is present and the property fails. If C=1 at time 310, the property would pass. If b=1 and c=0 at time 310, the property would continue to evaluate until it sees five consecutive 'b' or a c=1 before five consecutive 'b' are encountered. Or after five consecutive 'b' that there is a c=1 as shown in the previous part of the simulation log file.

Confusing? That could be the case at first. However, please see the next few applications and this concept will be clear. *This is one of the most useful operators in the language* and the better you understand it, the more productive you will be.

6.4.1 Application: Consecutive Repetition Range Operator

This application is again on the same line that we have been following. Reason to carry on with the same example is to show how specification can change around seemingly similar logic.

Property in Fig. 6.12 says that at $rose(tagError), check for tErrorBit to remain asserted until mCheck is asserted. If tErrorBit does not remain asserted until mCheck gets asserted, the property should fail.

So, at $rose(tagError) and one clock later we check to see that $rose(tErrorBit) occurs. If it does, then we move forward at the same time (##0) with tErrorBit[*1:$]. This says that we check to see that tErrorBit remains asserted consecutively (i.e. at every posedge clk) until the *qualifying event* $rose(mCheck) arrives.

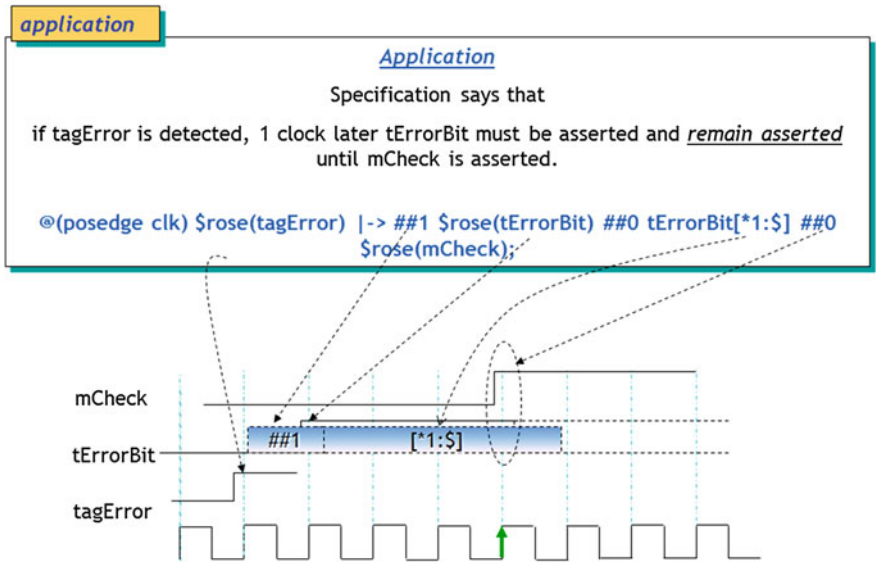


Fig. 6.12 [*m:n] Consecutive repetition range—application

In other words, the qualifying event is what makes consecutive range operator very meaningful as well as useful. Think of the qualifying event as the one that ends the property. This way, you can check for some expression to be true until the qualifying event occurs (Fig. 6.13).

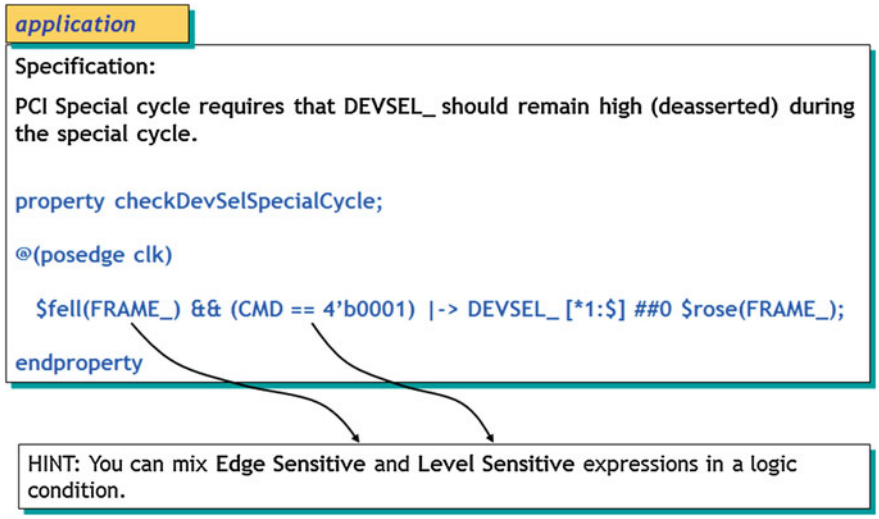


Fig. 6.13 [*m:n] Consecutive repetition range—application

A PCI cycle starts when FRAME_ is asserted (goes Low) and the CMD is valid. A CMD == 4'b0001 specifies the start of a PCI Special cycle. On the start of such a cycle (i.e. the antecedent being true), the consequent looks for DEVSEL_ to be high forever consecutively at every posedge clk until FRAME_ is de-asserted (goes High). This is by far the easiest way to check for an event/expression to remain true (and we do not know for how long) until another condition/expression is true (i.e. until what I call the qualifying event, is true).

Note also that you can mix edge sensitive and level sensitive expressions in a single logic expression. That is indeed impressive and useful.

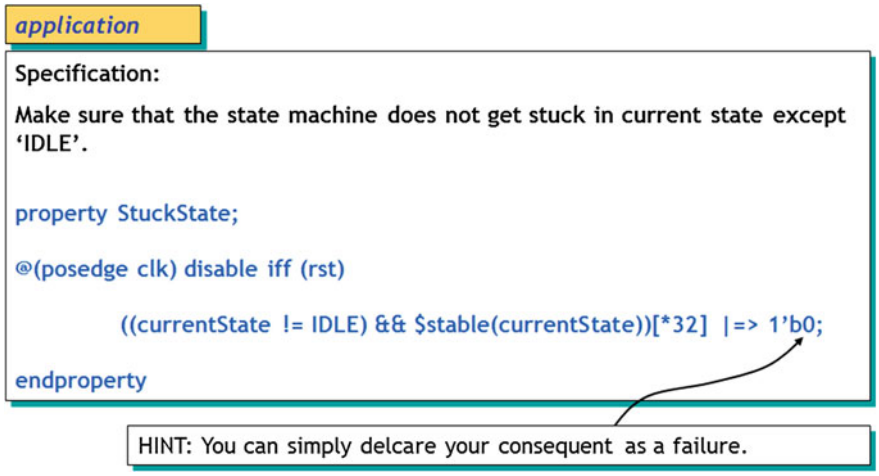


Fig. 6.14 [*m:n] Consecutive repetition range—application

Property in Fig. 6.14 states that if the currentState of the state machine is not IDLE and if the currentState remains stable for 32 clocks that the property should fail.

There are a couple of points to observe.

Note that the entire expression **((currentState !=IDLE) && $stable(currentState))** is checked for consecutive repetition of 32 times because we need to check at every clock for 32 clocks that the currentState is not IDLE and whatever state that existed in previous clock still remains the same (i.e. $stable). In other words, you have to make sure that within these 32 clocks, the current State does not go back to IDLE. If it does, then the antecedent fails and it will start all over again to check for this condition to be true (i.e. the antecedent to be true).

Note that if the antecedent is indeed true it would mean that the state machine is indeed stuck into the same state for 32 clocks. In such a case, we want to assertion to fire. That is taken care of by a hard failure in the consequent. We simply program consequent to fail without any pre-requisite.

As you notice, this property is unique in that the condition is checked for in the antecedent. The consequent is simply used to declare a failure (Fig. 6.15).

application

Specification:

Make sure that the state machine transitions for a given protocol in a specified manner

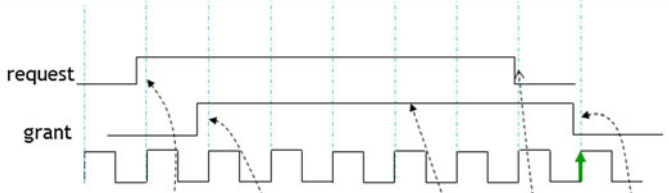
```
sequence checkReadStates;

  @(posedge clk) disable iff (rst)
  `readStart              ##1
  `readID         [*1:$]  ##1
  `readData       [*1:$]  ##1
  `readEnd        ;

endsequence
```

Fig. 6.15 [*m:n] Consecutive repetition range—application

This application states that the state machine matches the state transition specification. If we are in ‘readStart state that after 1 clock, the state machine should be in ‘readID state and stays in that state until the state machine reaches ‘readData state. It then is expected to stay in ‘readData state until ‘readEnd arrives.

Specification:

- When request is asserted that grant is asserted the very next clock.
  - *grant must have been de-asserted prior to it's assertion.*
- grant must remain asserted as long as request is asserted.
- grant must de-assert the very next clock after request is de-asserted.



application

```
property req_gnt;
 @(posedge clk)
$rose(request) |-> ##1 $rose(grant) ##0 grant[*1:$] ##0 $fell(request) ##1 $fell(grant);
endproperty

baseP: assert property (req_gnt) else $display($stime,,,"FAIL");
```

Fig. 6.16 Design application

In short, we have made sure that the state machine does not stray and do an illegal transition until it reaches 'readEnd.

Let us examine one more application as follows (Figs. 6.16 and 6.17).

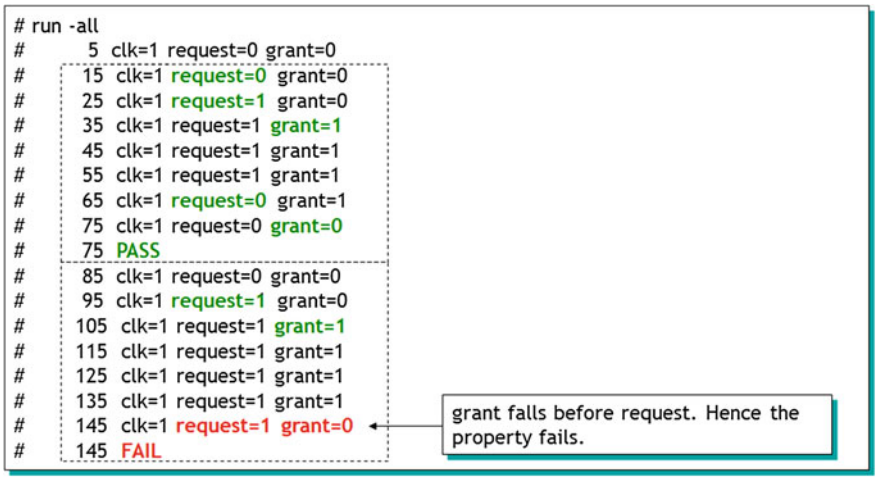


Fig. 6.17 Design application—simulation log

6.5 [=m]: Repetition Non-Consecutive

Non-consecutive repetition is another useful operator (just as the consecutive operator) and used very frequently. In many applications, we want to check that a signal remains asserted or de-asserted a number of clocks and that we need not know when exactly these transitions take place. For example (as we will see in Fig. 6.21), if there is a non-burst READ of length 8, that you expect 8 RDACK. These RDACK may come in a consecutive sequence *or not* (based on read latency). But you must have 8 RDACK before read is done.

In Fig. 6.18, property 'ab' says that if 'a' is sampled high at the posedge of clock that starting next clock, 'b' should occur twice not necessarily consecutively. They can occur any time after the assertion of 'a'. The interesting (and important) thing to note here is that even though the property uses non-overlapping implication operator (i.e. the first 'b' should occur 1 clock after 'a'=1), the first 'b' can occur *any time after* 1 clock after 'a' is found high. Not necessarily exactly 1 clock after 'a' !!!

In the simulation log, the first part shows that 'b' does occur 1 clock after 'a' and then is asserted again a few clocks later. This meets the property requirements and the assertion passes.

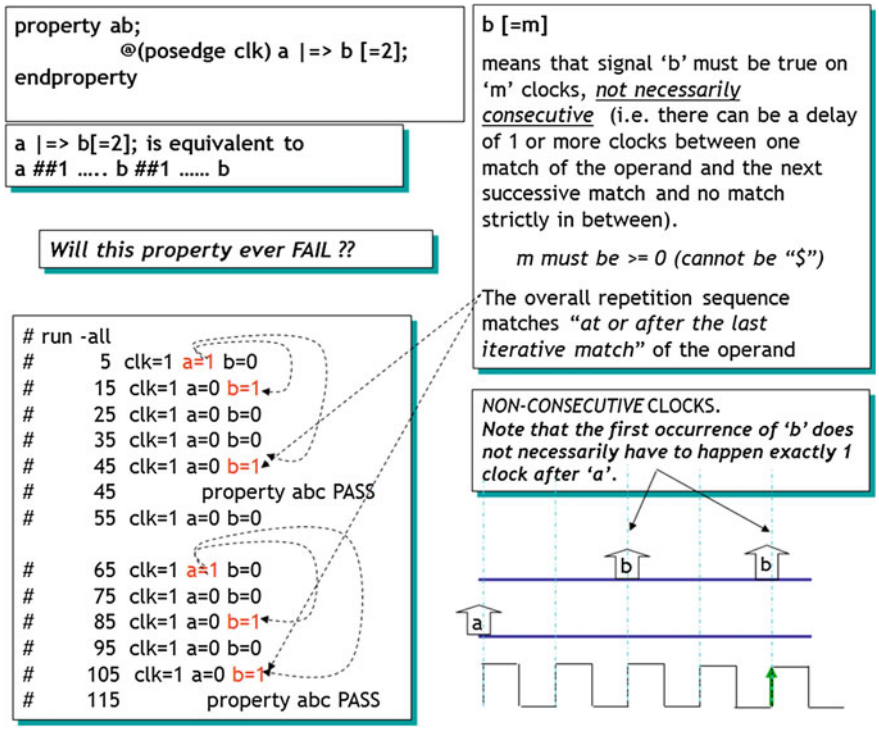


Fig. 6.18 Repetition non-consecutive operator—basics

But note that second part of the log. 'b' does –not- occur 1 clock after 'a', rather 2 clocks later. And then it occurs again a few clocks later. Even this behavior is considered to meet the property requirements and the assertion passes.

Based on the description above, do you think this property will ever fail? Please experiment and see if you can come up with the answer. It will also further confirm your understanding. Hint: There is no qualifying event after 'b[=2]'.

Continuing with the same analogy, refer to the example below. Here again, just like in the consecutive operator, the qualifying event (##1 C in the example below) plays a significant role.

The example in Fig. 6.19 is identical to the previous except for the '##1 C' at the end of the sequence. The behavior of 'a | =>b[=2]' is identical to what we have seen above. '##1 c' tells the property that after the last 'b', 'c' must occur once and then it can occur any time after one clock after the last 'b'. Note again that even though we have '##1 c', 'c' does *not* necessarily need to occur 1 clock after the last 'b'. It can occur after any # of clks after 1 clock after the last 'b'—as long as—no other 'b' occurs while we are waiting for 'c'. Confusing! Not really. Let us look at the simulation log in Fig. 6.19. That will clarify things.

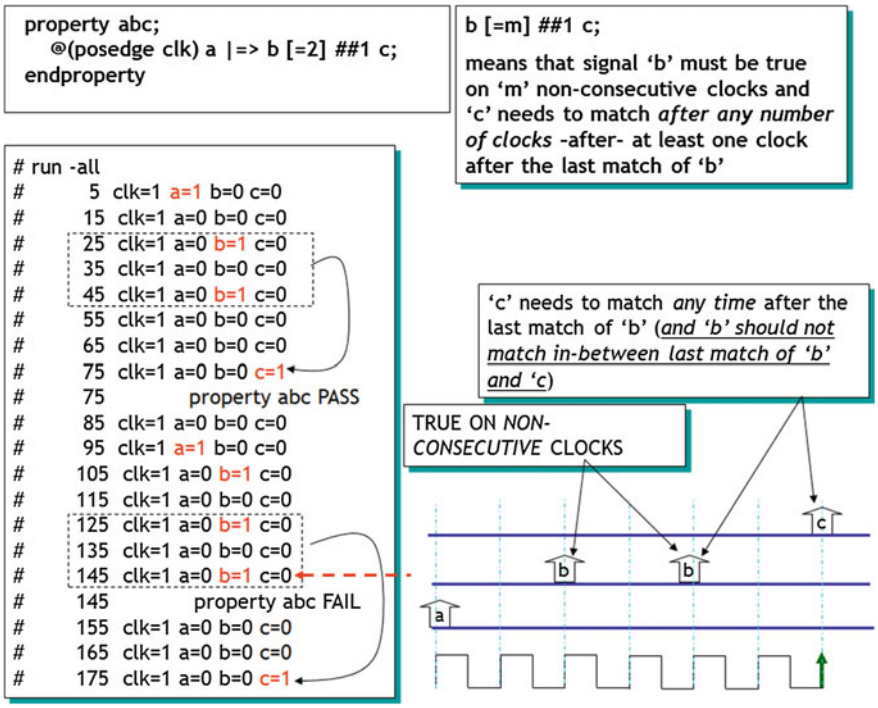


Fig. 6.19 Non-consecutive repetition operator—example

In the log, a=1 at time 5; b=1 at time 25 and then at 45. So far so good. We are marching along just as the property expects. Then comes in c=1 at time 75. That also meets the property requirement that 'c' occurs any time after last b=1. BUT note that *before* c=1 arrived at time 75, 'b' did not go to a '1' after its last occurrence at time 45. The property passes. Let us leave this at that for the moment. Now let us look at the second part of the log.

a=1 at time 95; then b=1 at 105 and 125; we are doing great. Now we wait for c=1 to occur any time after last 'b'. C=1 occurs at time 175. But the property fails before that!! What is going on? Note b=1 at time 145. That is not allowed in this property. The property expects a c=1 after the *last* occurrence of 'b' but *before* any other b=1 occurs. If another b=1 occurs *before* c=1 (as at time 145), then all bets are off. Property does not wait for the occurrence of c=1 and fails as soon as it sees this extra b=1. In other words, (what I call) the qualifying event "##1 c" encapsulates the property and strictly checks that b[=2] allows only two occurrences of 'b' before 'c' arrives.

6.6 [=m:n]: Repetition Non-Consecutive Range

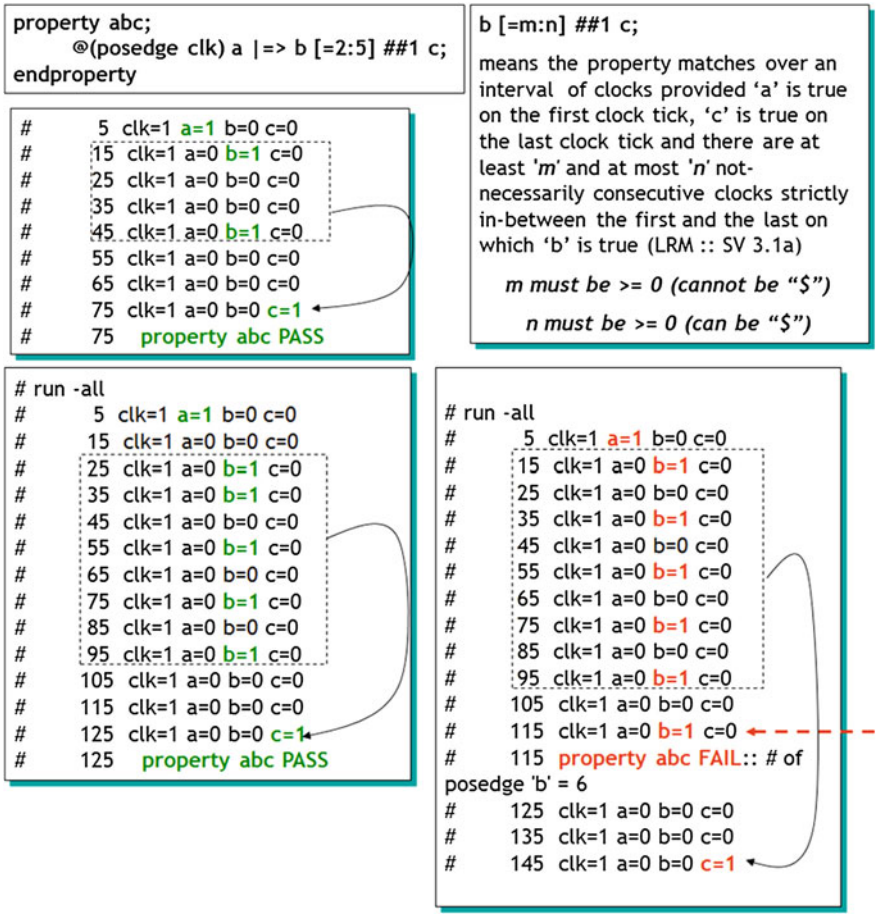


Fig. 6.20 Repetition non-consecutive range—basics

Property in Fig. 6.20 is analogs to the non-consecutive (non-range) property, except that this has a range. The range says (in the example above) that 'b' must occur minimum 2 times or maximum 5 times after which 'c' can occur one clock later any time and that no more than maximum of five occurrences of 'b' occur between the last occurrence of b=1 and c=1.

First simulation log (top left) shows that after a=1 at time 5, b occurs twice (the minimum # of times) at time 15 and 45 and then c=1 at time 75. Why didn't the property wait for 5 occurrences of b=1? That is because after the second b=1 at time 45, c=1 arrives at time 75 and this c=1 satisfies the property requirement of minimum of two b=1 followed by a c=1. The property passes and does not need to wait for any further b=1. In other words, the property starts looking for 'c=1' after

the minimum required (2) 'b==1'. Since it did find a 'c=1' after two 'b=1', the property ends there and passes.

Similarly the simulation log on bottom left shows that 'b' occurs 5 (max) times and then 'c' occurs without any occurrence of b. The property passes. This is how that works. As explained above, after two 'b=1', the property started looking for 'c==1'. But before the property detects 'c==1', it sees another 'b==1'. That's OK because 'b' can occur maximum of five times. So, after the third 'b==1', the property continues to look for either 'c==1' or 'b==1' until it has reached maximum of five 'b==1'. This entire process continues until five 'b's are encountered. Then the property simply waits for a 'c'. While waiting for a 'c' at this stage, if a 6th 'b' occurs, the property fails. This failure behavior is shown in simulation log in the bottom right corner of Fig. 6.20.

6.6.1 Application: Repetition Non-Consecutive Operator

Here is a practical example of using non-consecutive operator. The specs are provided in Fig. 6.21.

application

Specification:

- If nonBurst Read of length 8 is asserted that the RdAck must be asserted 8 times and ReadDone must be asserted anytime after the last Read and that there are no more RdAck's between the last RdAck and ReadDone.

```
property RdAckCheck (int length);

        @(posedge clk) nBurstRead  |=> RdAck [=length] ##1 ReadDone;

endproperty

aP: assert property (RdAckCheck (8));
```

Fig. 6.21 Repetition non-consecutive range—application

The property RdAckCheck will wait for nBurstRead to be high at the posedge clk. Once that happens, it will start looking for 8 RdAck before ReadDone comes along. If ReadDone comes in after 8 RdAck (and not 9) the property will pass. If ReadDone comes in before 8 RdAck come in the property will fail. Note that this will guarantee that the non-burst protocol is completely adhered to.

Following is an interesting example, just for fun… (Fig. 6.22).

```
property abc;
        @(posedge clk) a |=> b [=0:$]
##1 c;
endproperty
```

b [=0:$] ##1 c;

means that the signal 'b' should be true either at no time 1 clock (after 'a' is true in this example) or it can be true infinite times until 'c' is asserted.

Will this property ever fail??

```
# run -all
#        5  clk=1 a=1 b=0 c=0
#       15  clk=1 a=0 b=0 c=1
#       15    property abc PASS

#       35  clk=1 a=1 b=0 c=0
#       45  clk=1 a=0 b=0 c=0
#       55  clk=1 a=0 b=1 c=0
#       65  clk=1 a=0 b=0 c=1
#       65    property abc PASS

#       75  clk=1 a=1 b=0 c=0
#       85  clk=1 a=0 b=1 c=1
#       85    property abc PASS
#       95  clk=1 a=0 b=1 c=1
```

Fig. 6.22 Repetition non-consecutive range—[= 0:$]

The first case is interesting. At time 5 'a' is 1 (antecedent is true) which triggers the consequent. At time 15, c=1 and the property passes. But there was no occurrence of 'b'. b[=0] is an empty sequence which states that 'b' should *not* occur. We'll discuss empty sequences later in the book. The log from time 35–65 is quite straightforward. 'a==1' at time 35; 'b==1' at time 55 and 'c==1' at time 65. Since the property states b[=0:$] and since 'b' did occur once followed by a 'c', the property passes.

But let us examine the log from time 75. At time 75, a=1 so the consequent fires. At time 85, both b=1 and c=1 and property passes! How? Note again that b[=0] part of the b[=0:$] range states that 'b' may never occur. That property is satisfied at time 75 (i.e. 'b' does not occur) and 1 clock later 'c' arrives, hence the property passes. Once you learn a bit more about the empty sequences, you will better understand this example. But the point here is that you need to be careful using the minimum and maximum range in an operator. The results may not be that apparent.

Empty sequences are discussed in Sect. 14.6.

6.7 [->m] Non-Consecutive GoTo Repetition Operator

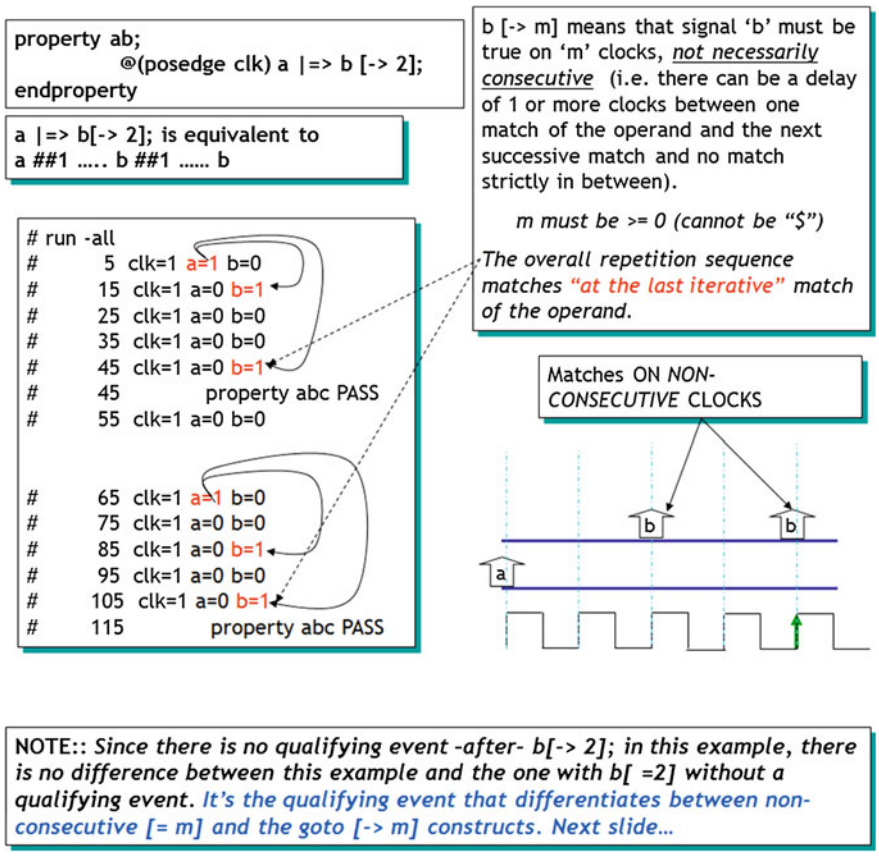


Fig. 6.23 GoTo non-consecutive repetition—basics

This is the so-called non-consecutive goto operator! Very similar to [=m] non-consecutive operator. Note the symbol difference. The goto operator is [->2].

In Fig. 6.23, b[->2] acts exactly the same as b[=2]. So, why bother with another operator with the same behavior? It is the *qualifying event* that makes the difference. Recall that the qualifying event is the one that comes after the non-consecutive or the 'goto' non-consecutive operator. I call it qualifying because it is *the end event* that qualifies the sequence that precedes for final sequence matching.

In Figure 6.24, we have the so-called qualifying event '##1 c'. The property says that on finding a=1 at posedge clk, b must be true 2 times (1 clock after a=1) non-consecutively and 'c' must occur *exactly* 1 clock after the last occurrence of 'b'. In contrast, with "b[=2] ##1 c", 'c' could occur *any time* after 1 clock after the last occurrence of 'c'. That is the difference between [=m] and [->m].

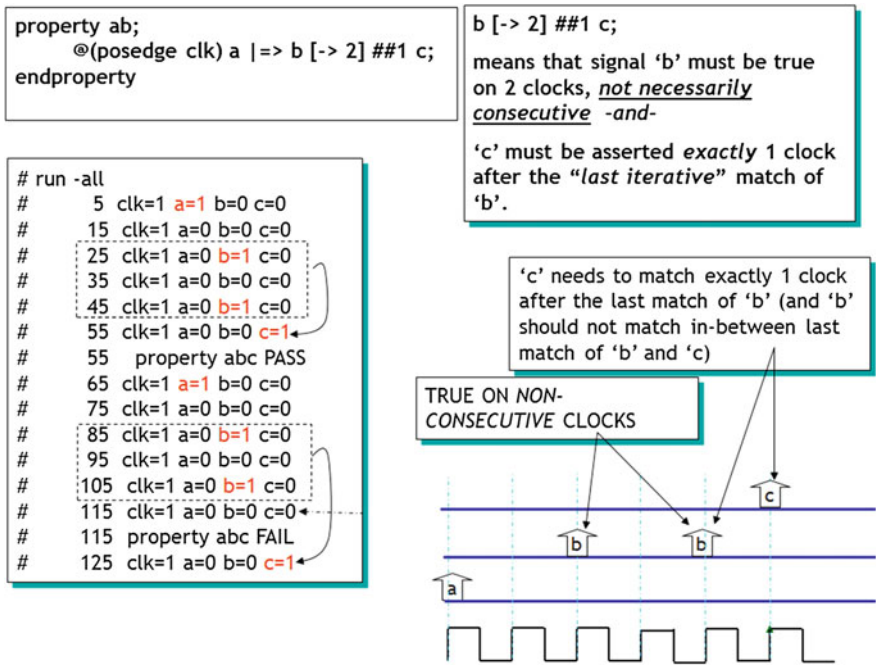


Fig. 6.24 Non-consecutive repetition—example

The simulation log in Fig. 6.24 shows a PASS and a FAIL scenario. PASS scenario is quite clear. At time 5, a==1, then two non-consecutive 'b' occur and then *exactly* 1 clock after the last 'b=1', 'c=1' occurs. Hence, the property passes. The FAIL scenario shows that after two occurrences of b==1, c==1 does *not* arrive *exactly* 1 clock after the last occurrence of b=1. That is the reason the b[->2] ##1 c check fails.

6.8 Difference Between [=m:n] and [->m:n]

The simulation log in Fig. 6.25 is quite self-explaining. The left and the right side properties are identical except that the LHS uses [=2:5] and RHS uses [->2:5]. The LHS log, i.e. the one for b[=2:5] PASSes while the one for b[->2:5] fails because according to the semantics of "b[->2:5] ##1 c', 'c' must arrive exactly 1 clock after the last occurrence of 'b'.

Now here is a very important point. Note that 'c' is expected to come in 1 clk after the last occurrence of b=1 because of '##1 c'. But what if you have '##2 c' in the property?

b[=m] ##2 C : This means that after 'm' non-consecutive occurrence of 'b', 'c' can occur any time *after* 2 clocks. If 'c=1' arrives before 2 clocks, the property will fail. b[->m]##2 c: This means that after 'm' non-consecutive occurrence of 'b', 'c' must occur *exactly* after 2 clocks. No more no less.

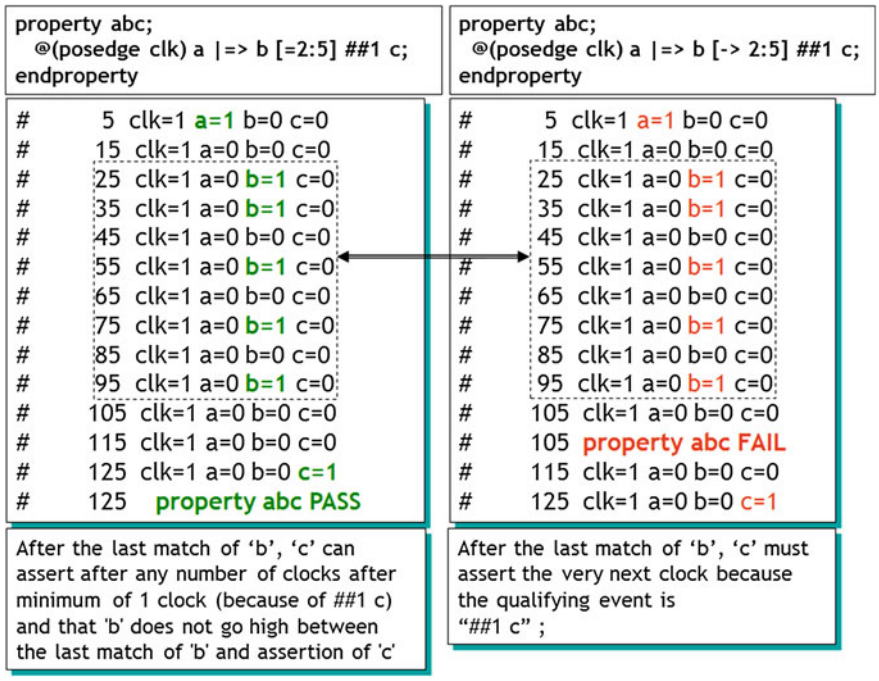


Fig. 6.25 Difference between [=m:n] and [->m:n]

6.8.1 Application: GoTo Repetition—Non-Consecutive Operator

The application says that at the rising edge of 'req', after 1 clock (because of non-overlapping operator) 'ack' must occur once and that it must de-assert (go low) exactly 1 clock after its occurrence. If 'ack' is not found de-asserted (low) exactly 1 clock after the assertion of 'ack', the property will fail (Fig. 6.26).

6.9 sig1 *Throughout* seq1

The 'throughout' operator makes it that much easier to test for condition (signal or expression) to be true throughout a sequence. Note that the LHS of 'throughout'

application

Specification:

- For every 'req' you must get *at least* 1 'ack' and 'ack' must clear the next clock.

```
property ReqAckCheck;
        @(posedge clk) $rose(req) |=> ack[->1] ##1 !ack;
endproperty
aP: assert property (reqAckCheck);
```

Fig. 6.26 GoTo repetition—non-consecutive operator—application

operator can only be a signal or an expression, but it cannot be a sequence (or subsequence). The RHS of 'throughout' operator can be a sequence. So, what if you want a sequence on the LHS as well? That is accomplished with the 'within' operator, discussed right after 'throughout' operator (Fig. 6.27).

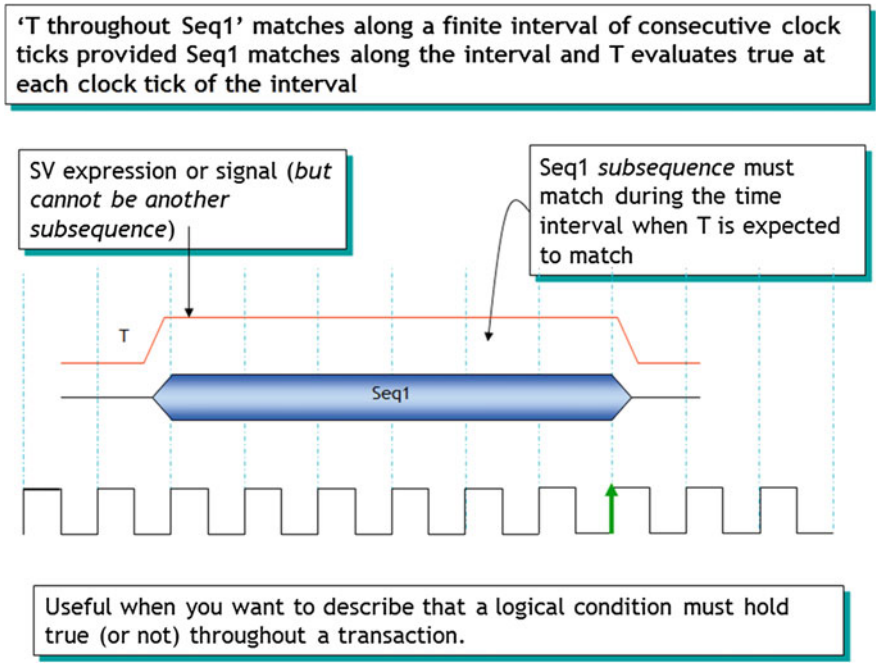


Fig. 6.27 sig1 *throughout* seq1

Let us examine the application in Fig. 6.28 which will help us understand the throughout operator.

6.9.1 Application: sig1 Throughout seq1

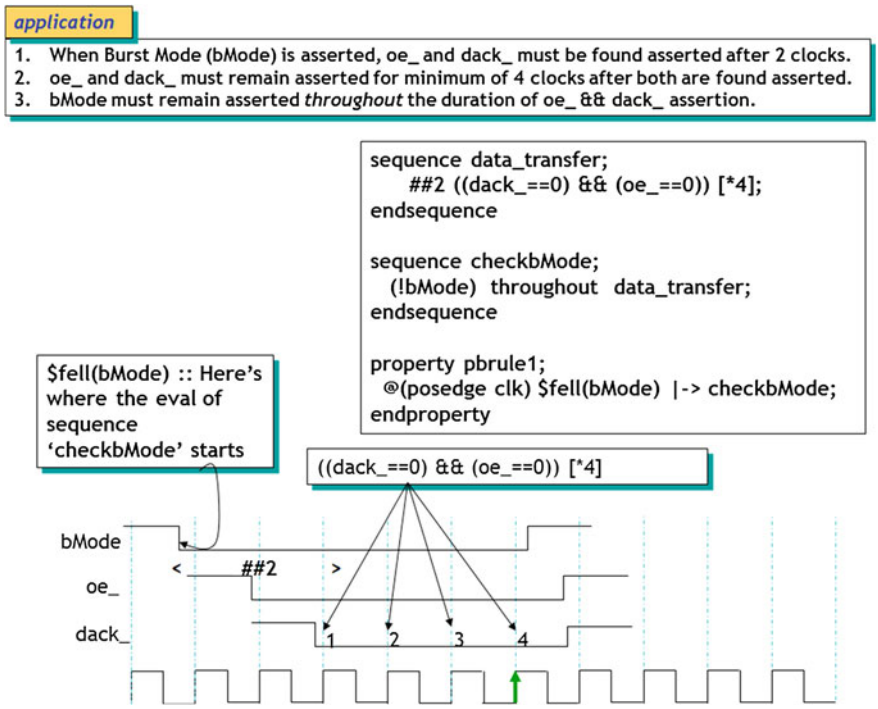


Fig. 6.28 sig1 *throughout* seq1—application

In Fig. 6.28 the antecedent in property pbrule1 requires bMode (burst Mode) to fall. Once that is true, it requires checkbMode to execute.

checkbMode makes sure that the bMode stays low 'throughout' the data_transfer sequence. Note here that we are, in a sense, making sure that the antecedent remains true through the checkbMode sequence. If bMode goes high before data_transfer is over, the assertion will fail. The data_transfer sequence requires both dack_ and oe_ to be asserted (active low) and to remain asserted for four consecutive cycles. Throughout the data_transfer, burst mode (bMode) should remain low.

There are two simulation logs presented in Fig. 6.29. Both are for FAIL cases! FAIL cases are more interesting than the PASS cases, in this example! The first simulation log (left hand side) shows $fell(bMode) at time 20. Two clocks later at time 40, oe_=0 and dack_=0 are detected. So far so good. oe_ and dack_ retain

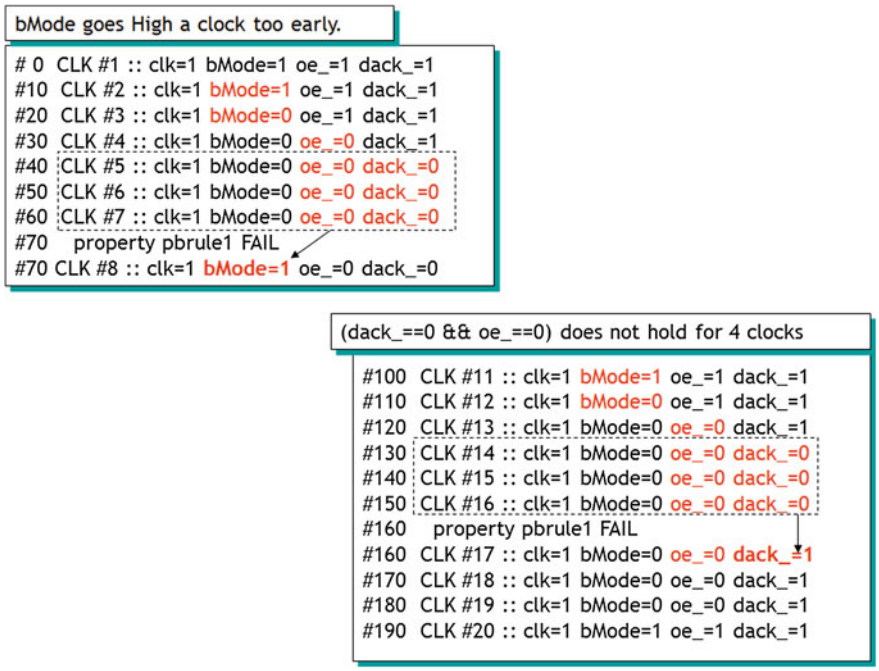


Fig. 6.29 sig1 throughout seq1—application

their state for 3 clocks That's good too. But in the 4th cycle (time 70), bMode goes high. That's a violation because bMode is supposed to stay low throughout the data-transfer sequence, which is 4 clocks long.

The second simulation log (Right hand side) also follows the same sequence as above but after three consecutive clocks that the oe_ and dack_ remain low, dack_ goes high at time 160. That is a violation because data_transfer (oe_=0 and dack_=0) is supposed to stay low for four consecutive cycles.

This also points to a couple of other important points:

(1) Both sides of the throughout operator must meet their requirements. In other words, either the LHS or the RHS of the throughout sequence fails that the assertion will fail. Many folks assume that since bMode is being checked to see that it stays low (in this case), only if bMod'e fails that the assertion will fail. Not true as we see from the two failure logs.
(2) Important Point: In order to make it easier for the reader to understand this burst mode application, I broke it down into two distinct subsequences. But what if someone just gave you the timing diagram and asked you to write assertions for it?

Break down any complex assertion requirement into smaller chunks. This is probably the most important advice I can part to the reader. If you look at the

entire AC protocol (the timing diagram) as one monolithic sequence, you will indeed make mistakes and spend more time debugging your own assertions then debugging the design under test.

Exercise: How would you model this application using a consecutive repetition [*m] operator? Please experiment to solidify your concepts of both the throughout and the [*m] operators.

6.10 seq1 *within* seq2

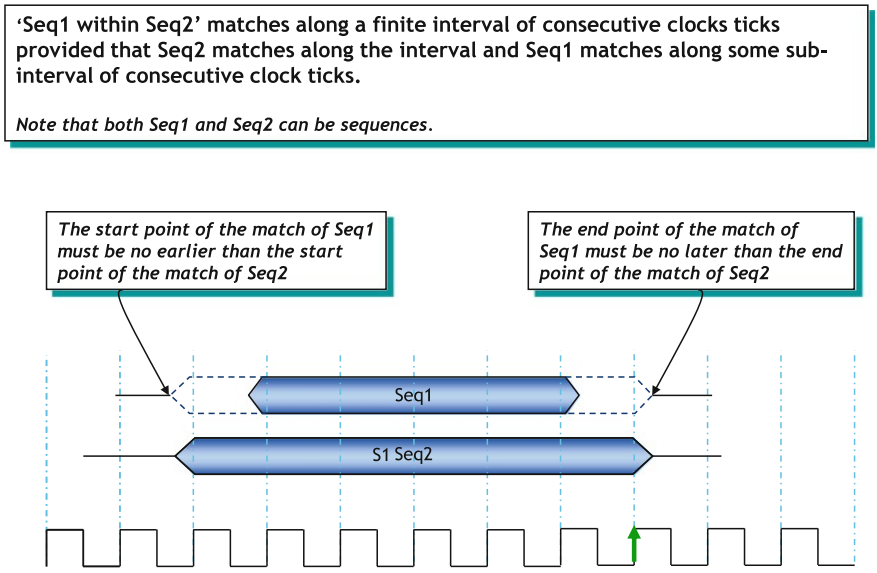


Fig. 6.30 seq1 within seq2

Analogous to 'throughout', the 'within' operator sees if one sequence is contained within or of the same length as another sequence. Note that the 'throughout' operator allowed only a signal or an expression on the LHS of the operator. 'within' operator allows a sequence on both the LHS and RHS of the operator.

The property with 'within' ends when the larger of the two sequences end, as shown in the (Fig. 6.30).

Let us understand 'within' operator with the application in Fig. 6.31.

6.10.1 Application: seq1 within seq2

Specification:
- Assertion of burst Mode (bMode) requires that Master Tx and Target Ack cycles follow the protocol below.
- Master Trx: mtrx must assert the clock after bMode and remains asserted for 9 clocks.
- Target Ack: tack must remain asserted for 7 clocks *within* mtrx transaction.

```
sequence stack;
  $fell(tack) ##0 !tack[*7];
endsequence

sequence smtrx;
  $fell (mtrx) ##0 (!mtrx[*9]) ;
endsequence

property pwin;
  @(posedge clk)  $fell(bMode) |=> stack within smtrx;
endproperty
```

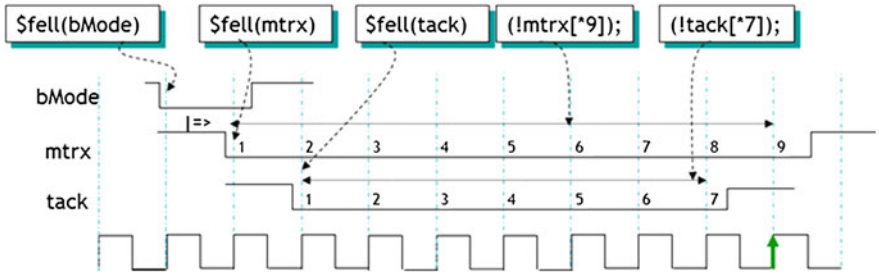


Fig. 6.31 seq1 *within* seq2—application

In Fig. 6.31, we again tackle the nasty protocol of burst mode! When burst mode is asserted, the master transmit (smtrx) must remain asserted for 9 clocks and the Target Ack (tack) must remain asserted for 7 clocks and that the 'tack' sequence occurs within the 'smtrx' sequence. This makes sense because from the protocol point of view, the target responds only after the master starts the request and the master completes the transaction after target is done.

In Fig. 6.31, the assertion of bMode ($fell(bMode)) implies that 'stack' is valid 'within' 'smtrx'. Now, carefully see the implication property "@ (posedge clk) $fell(bMode) |=> stack **within** smtrx;"

LHS and RHS sequences start executing once the consequence fires. 'stack' will evaluate to see if it is condition remains true and 'smtrx' starts its own evaluation.

At the same time, the 'within' operator continually makes sure that 'stack' is contained with 'smtrx'. The annotations in Fig. 6.31 show how the property handles different parts of the protocol. Simulation logs are presented in Fig. 6.32.

6.10.2 'within' Operator PASS CASES

Fig. 6.32 *within* operator—simulation log example—PASS cases

On the left hand side of Fig. 6.32, bMode is '1' at time 0 (not shown) and at time 10, it goes to '0'. That satisfies $fell(bMode). After that the consequent starts execution. Both 'stack' and 'smtrx' sequences start executing. As shown in the left side simulation log, 'mtrx' falls and stays low for 9 clocks, as required. 'tack' falls after 'mtrx' falls, stays low for 7 clocks and goes high the same time when 'mtrx' goes high (i.e. both sequences end at the same time). In other words, 'tack' is contained within 'mtrx'. This satisfies the 'within' operator requirement and the property passes. Note that the operator 'within' can have either sequences start or end at the same time. Similarly, the right side log shows that both sequences start at the same time and 'tack' is contained within 'mtrx' and the property passes. Now let us look at fail cases.

6.10.3 'within' Operator: FAIL CASES

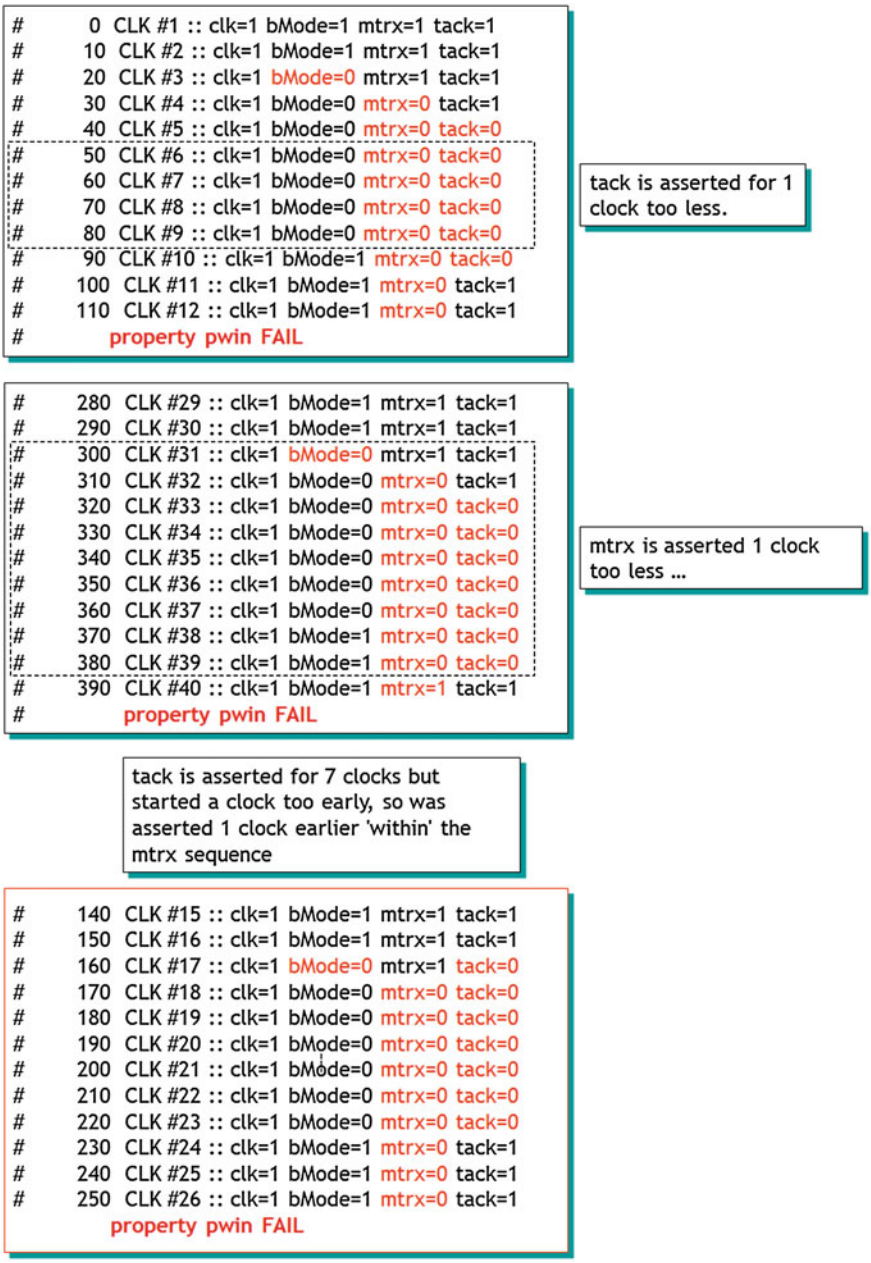


Fig. 6.33 *within* operator—simulation log example—FAIL cases

The simulation logs show different cases of failure. In the top side, 'tack' is indeed contained within 'mtrx', but 'tack' does not remain asserted for required 7 clocks and the property fails (Fig. 6.33).

In the middle log, again 'tack' is contained within 'mtrx' but this time around, 'mtrx' is asserted 1 clock too less.

The log at the bottom shows both 'tack' and 'mtrx' asserted for their required clks but 'tack' starts one clk before the falling edge of 'mtrx', thus violating the 'within' semantics. Sequences on either side of 'within' can start at the same time or end at the same time but the sequence that is to be contained within the larger sequence cannot start earlier or end later that of the larger sequence.

Another important point to note from these simulation logs is that the *property ends when the larger of the two sequences end*. In our case, the property does not end as soon as there is a violation on 'stack'. It waits for 'smtrx' to end to make a judgment call on pass/fail of the property 'pwin'.

6.11 seq1 and seq2

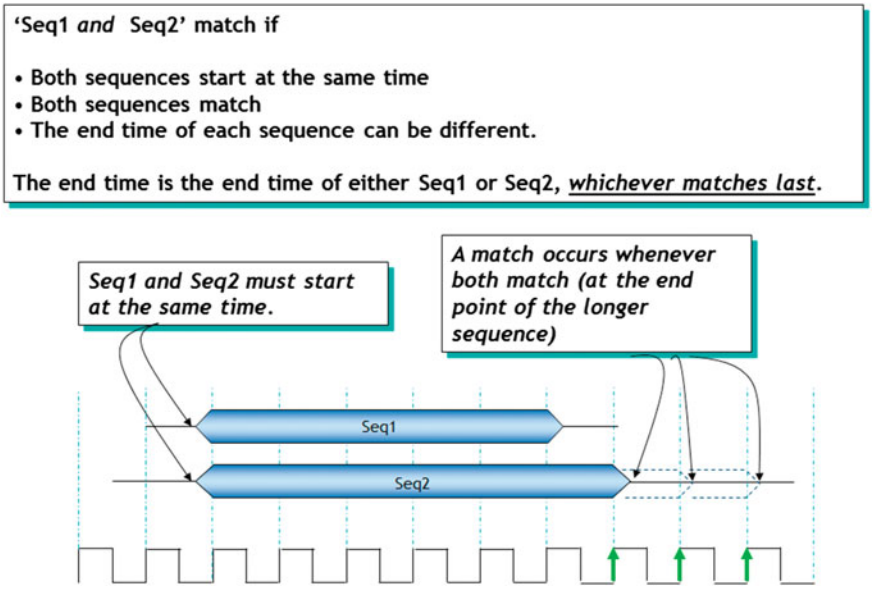


Fig. 6.34 seq1 *and* seq2—Basics

As the name suggests, 'and' operator expects both the LHS and RHS side of the operator 'and' to evaluate to true. It does not matter which sequence ends first as long as both sequences meet their requirements. The property ends when the longer of the two sequences ends. *But note that both the sequences must start at the same time* (Fig. 6.34).

The 'and' operator is very useful, when you want to make sure that certain concurrent operations in your design, start at the same time and that they both complete satisfactorily. As an example, in the processor world, when a Read is issued to L2 cache, L2 will start a tag match and issue a Read at the same time, in anticipation that the tag may not match. If there is a match, it will abort the Read. So, one sequence is to start tag compare while other is to start a Read (ending in Read Complete or Abort). The Read sequence is designed such that it will abort as soon as there is a tag match. This way we have made sure that both sequences start at the same time and that both do end. Let us look at the following cases to clearly understand 'and' semantics. The figures are self-explaining with annotation within the figures (Figs. 6.35 and 6.36).

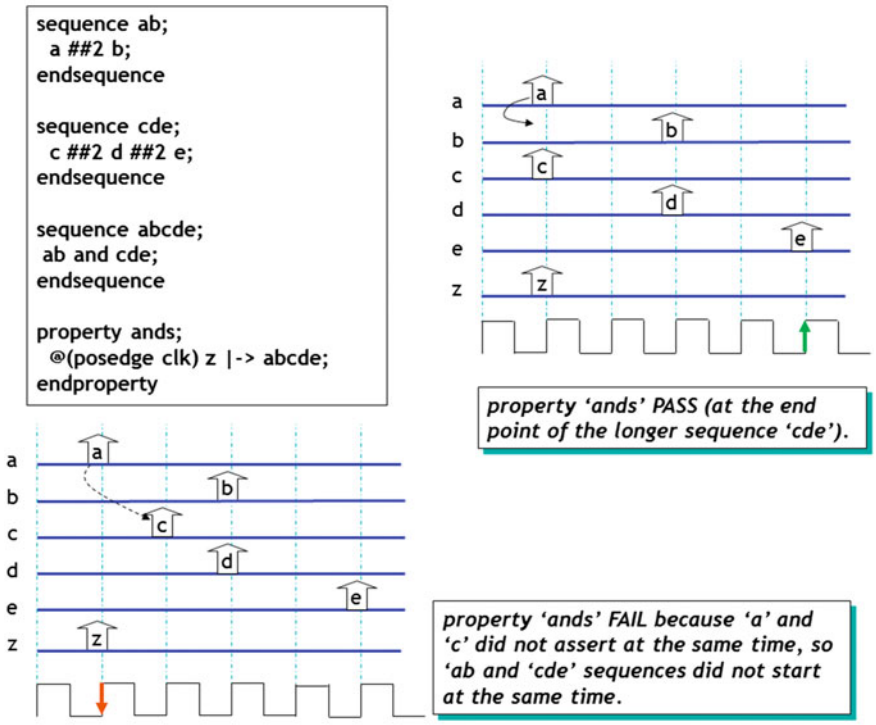


Fig. 6.35 *and* operator—application

6.11.1 Application: ‘and’ Operator

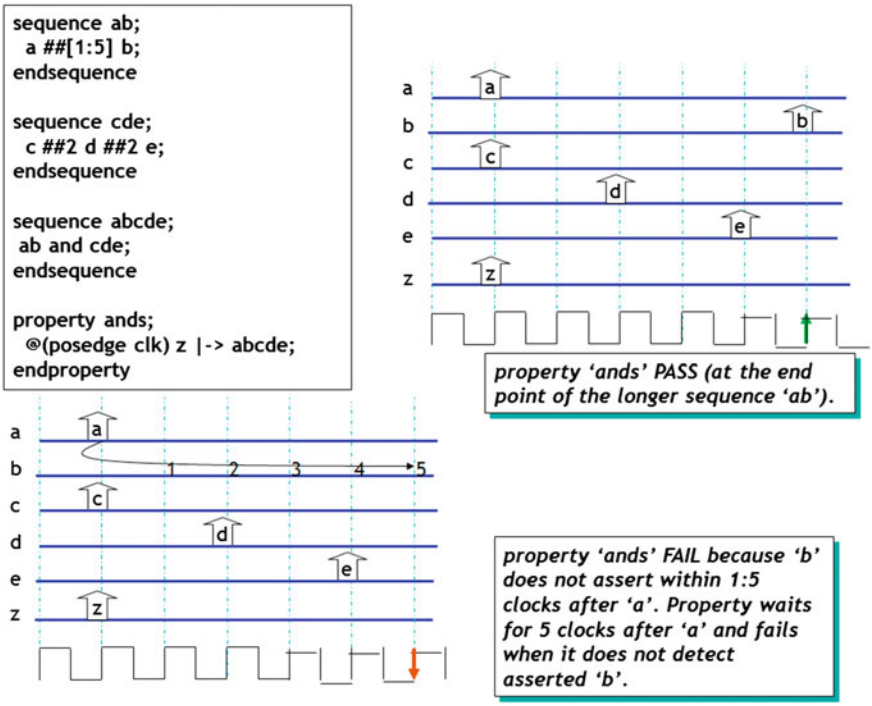


Fig. 6.36 *and* operator—application-II

In Fig. 6.37, we ‘and’ two expressions in a property. In other words, as noted before, an ‘and’ operator allows a signal, an expression or a sequence on both the LHS and RHS of the operator. The simulation log is annotated with pass/fail indication.

6.12 seq1 ‘or’ seq2

‘or’ of two sequences means that when either of the two sequences match its requirements that the property will pass Please refer to Fig. 6.38 and examples that follow to get a better understanding.

The feature to note with ‘or’ is that as soon as either of the LHS or RHS sequence meets its requirements that the property will end. This is in contrast to ‘and’ where only after the longest sequence ends that the property is evaluated.

```
property ands;
  @(posedge clk) z |-> (a==b) and (c==d);
endproperty
```

```
# run -all
#        5  CLK # 1 :: clk=1 z=0 a=0 b=0 c=0 d=0
#       15  CLK # 2 :: clk=1 z=0 a=0 b=0 c=0 d=0
#       25  CLK # 3 :: clk=1 z=1 a=1 b=1 c=0 d=0
#       25    property ands PASS

#       35  CLK # 4 :: clk=1 z=0 a=0 b=0 c=1 d=1
#       45  CLK # 5 :: clk=1 z=1 a=1 b=1 c=1 d=1
#       45    property ands PASS

#       55  CLK # 6 :: clk=1 z=0 a=0 b=1 c=0 d=1
#       65  CLK # 7 :: clk=1 z=1 a=1 b=0 c=1 d=1
#       65    property ands FAIL

#       75  CLK # 8 :: clk=1 z=1 a=1 b=1 c=0 d=1
#       75    property ands FAIL
```

Note that you can do an 'and' of sequences or expressions or a combination of the two.

Fig. 6.37 *and* of expressions

'Seq1 *or* Seq2' match if

- operand 'or' is used when at least one of the two operand sequences is expected to match.

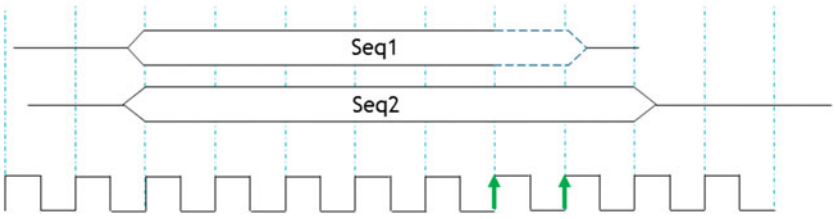


Fig. 6.38 seq1 or seq2—basics

Note also that if the shorter of the two sides fails, the sequence will continue to look for a match on the longer sequence. Following examples make all this clear.

6.12.1 Application: or Operator

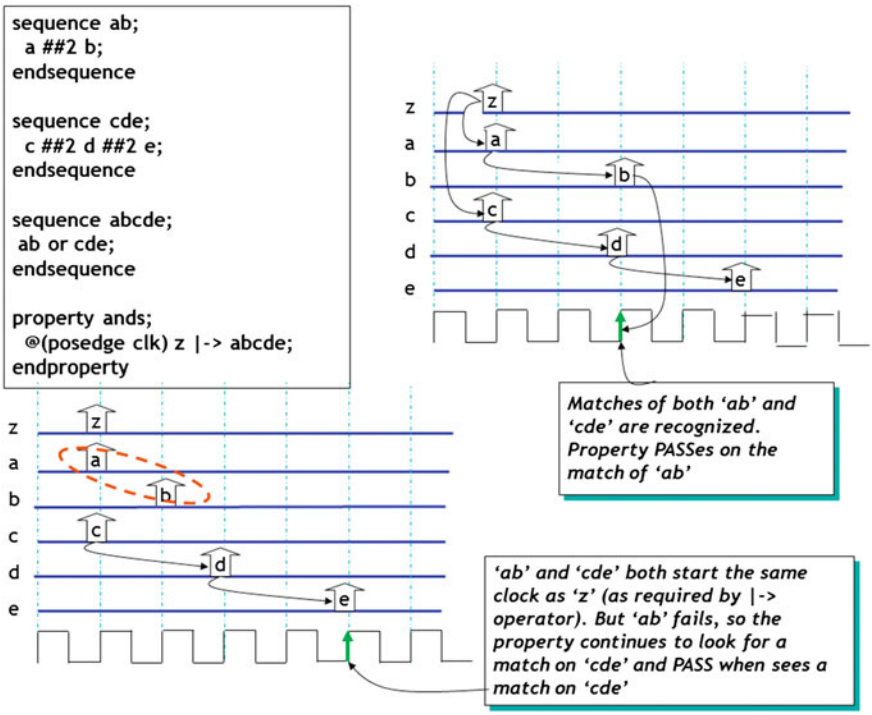
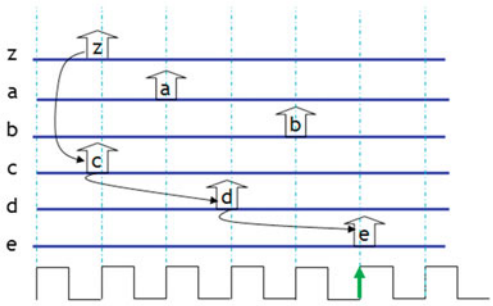


Fig. 6.39 *or* operator—application

A simple property is presented in Fig. 6.39. Different cases of passing of the property are shown. On the top right of the figure, both 'ab' and 'cde' sequences start at the same time. Since this is an 'or', as soon as 'ab' completes, the property completes and passes. In other words, the property does not wait for 'cde' to complete anymore.

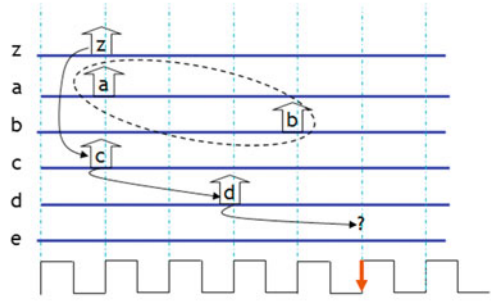
On the bottom left corner, we see that 'ab' sequence fails. However, since this is an 'or' the property continues to look for 'cde' to be true. Well, 'cde' does turn out to be true and the property passes (Figs. 6.40, 6.41 and 6.42).

```
sequence ab;
  a ##2 b;
endsequence

sequence cde;
  c ##2 d ##2 e;
endsequence

sequence abcde;
 ab or cde;
endsequence

property ands;
  @(posedge clk) z |-> abcde;
endproperty
```



Here 'a' is asserted 1 clock later and 'ab' does satisfy it's requirement, but 'a' was not asserted the same time as 'z' (as required by overlap implication). however, 'c' was indeed asserted when 'z' was asserted, the property is looking for 'cde' to match. Since 'cde' does match, the property passes at the end of 'cde' (and not at the end of 'ab').

```
sequence ab;
  a ##2 b;
endsequence

sequence cde;
  c ##2 d ##2 e;
endsequence

sequence abcde;
 ab or cde;
endsequence

property ands;
  @(posedge clk) z |-> abcde;
endproperty
```



Here, 'ab' does not match; but property keeps looking to see if 'cde' matches. But when 'e' does not follow 2 clocks after d, 'cde' also fails and the property FAILs at that time.

Fig. 6.40 or operator—application II

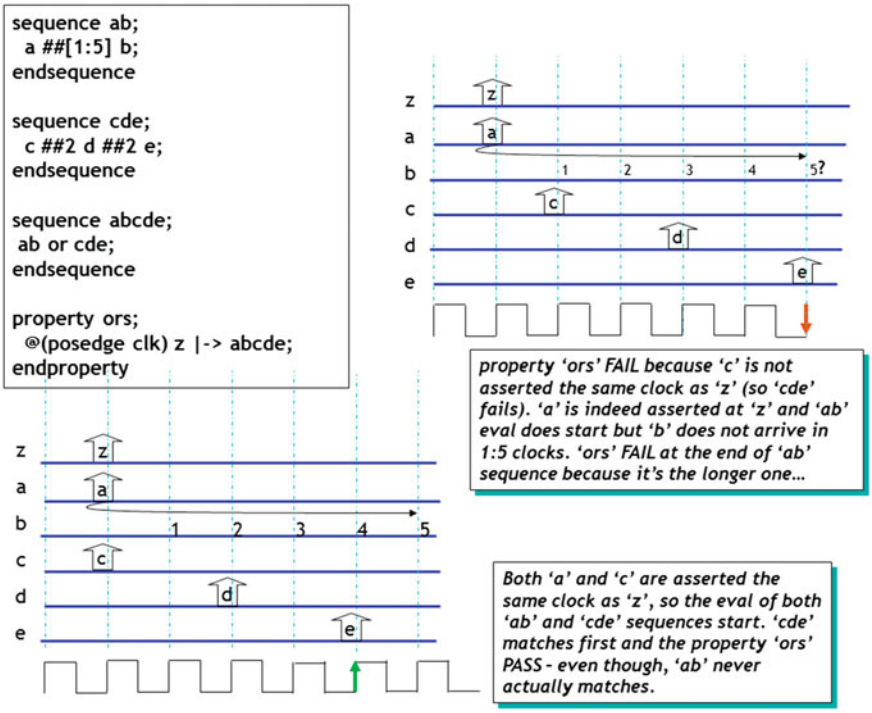


Fig. 6.41 or operator—application III

6.13 seq1 'intersect' seq2

So, with 'throughout', 'within', 'and' and 'or' operators who needs another operator that also seem to verify that sequences match? (Fig. 6.43).

'throughout' or 'within' or 'and' or 'or 'does *not* make sure that both the LHS and RHS sequences of the operator are exactly the same. They can be of the same length but the operators do not care as long as the signal/expression or sequence meets their requirements. That's where 'intersection' comes into picture. It makes sure that the two sequences indeed start at the same time *and* end at the same time and satisfy their requirements. In other words, they intersect.

As you can see, the difference between 'and' and 'intersect' is that 'intersect' requires both sequences to be of the same length and that they both start at the same time and end at the same time, while 'and' can have the two sequences of different lengths. I have shown that difference with timing diagrams further down the chapter. But first, some simple examples to understand 'intersect' better.

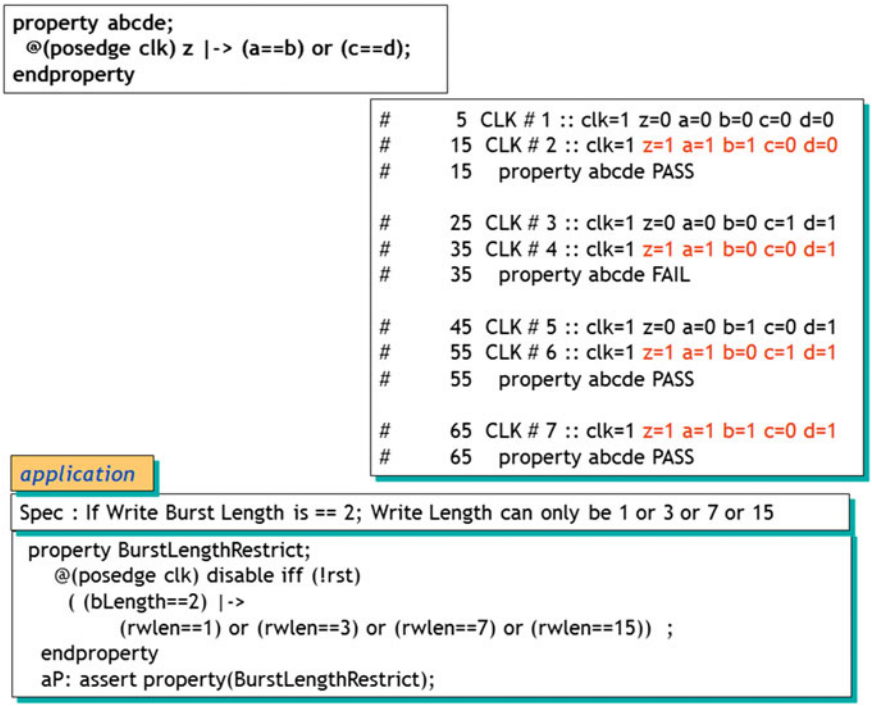


Fig. 6.42 *or* of expressions

6.14 Application: 'intersect' Operator

Figure 6.44 shows two cased of failure with the 'intersect' operator.

Property 'isect' says that if 'z' is sampled true at the posedge clk that sequence 'abcde' should be executed and hold true. I have broken down the required sequence into two subsequences. Sequence 'ab' requires 'a' to be true at posedge clk and then 'b' be true any time from 1 to 5 clks. Sequence 'cde' is a fixed temporal domain sequence which requires c to be true at posedge clk, then d to be true 2 clocks later and 'e' to be true 2 clocks after 'd'.

Top Right timing diagram in Fig. 6.44 shows that both 'ab' and 'cde' meet their requirements but the property fails because they both do not end at the same time (even though they start at the same time). Similarly, the bottom left timing diagram shows that both 'cde' and 'ab' meet their requirements but don't end at the same time and hence the assertion fails.

In Fig. 6.45 we show a PASS case of the same property (repeated here for the sake of convenience). Both 'ab' and 'cde' meet their requirements and end at the same time. Hence the assertion passes.

Now let's look at the example in Fig. 6.46. This one does not use a range operator in sequence 'ab' (as in the above example). It is obvious that without the

'Seq1 *intersect* Seq2' match if

- Both sequences start at the same time
- Both sequences must match
- *The lengths of the two matches of the operand sequences must be the same.*

The end time is when both sequences match and end at the same time.

The main difference between 'and and 'intersect' is the requirement on the length of the two sequences. For 'and' each sequence can be of any length. For 'intersect' they must be of the same length.

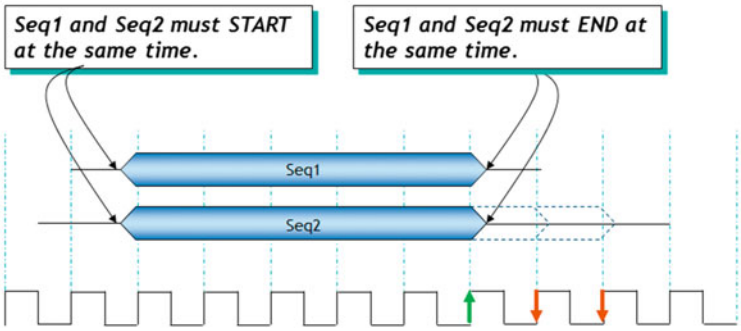


Fig. 6.43 seq1 intersect seq2

range operator that the two sequences with fixed lengths and ending at different times, the intersect property will never pass. *Hence, it makes sense to use sub-sequences with a range while using an 'intersect' operator.*

6.14.1 Application: Intersect Operator (Interesting Application)

OK, I admit this property could have been written much simpler, as

```
@ (posedge clk) $rose(Retry) |-> Retry ##[1:4] $rose(dataRead);
```

So, why are we making it complicated? I just want to highlight an interesting way to use 'intersect' (Fig. 6.47).

When $rose(Retry) is true, the consequent executes. The consequent uses 'intersect' between 'true[*1:4] and (Retry ##[1:$] $rose(dataRead)). The LHS of 'intersect' says that it will be True for consecutive 4 cycles. The RHS says that Retry should occur from now until forever but only until $rose(dataRead). Now, recall that 'intersect' requires both the LHS and RHS to be of 'same' length.

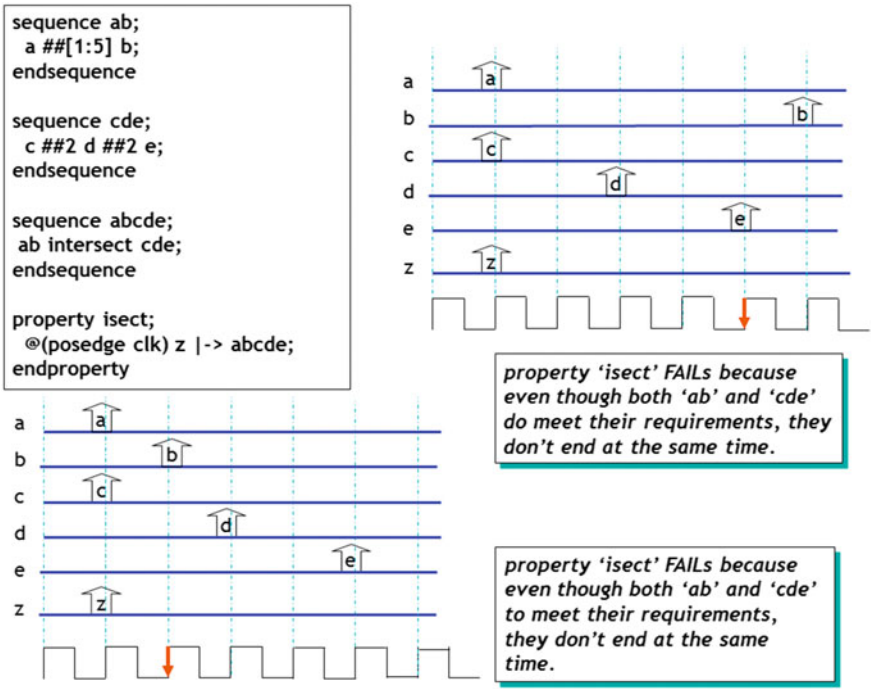


Fig. 6.44 seq1 'intersect' seq2—application

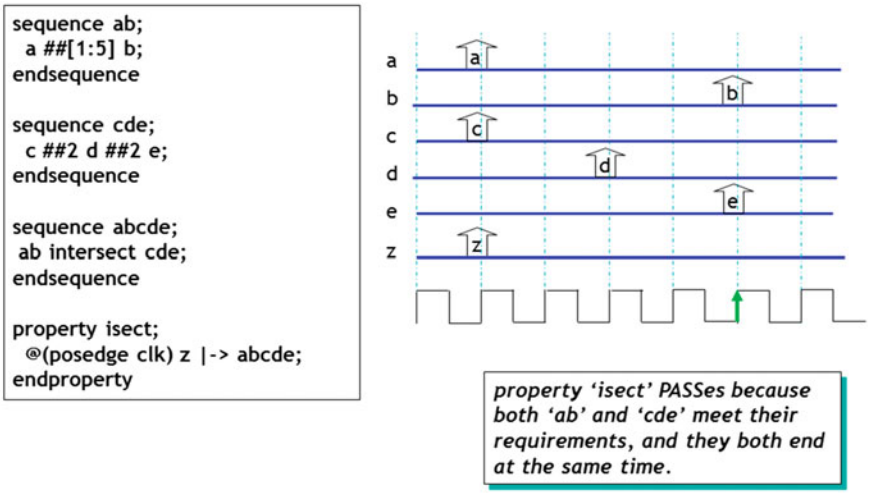


Fig. 6.45 seq1 intersect seq2 – Application II

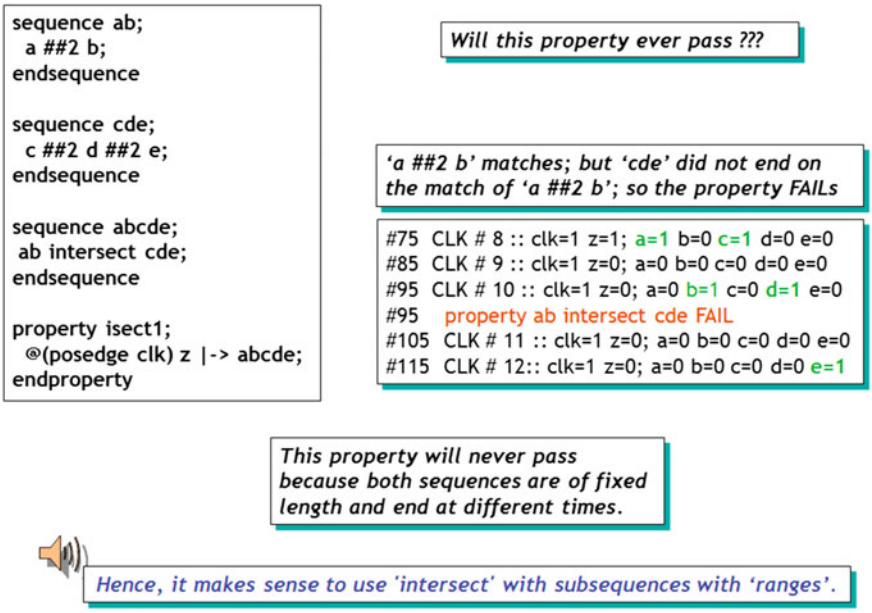


Fig. 6.46 *intersect* makes sense with subsequences with ranges

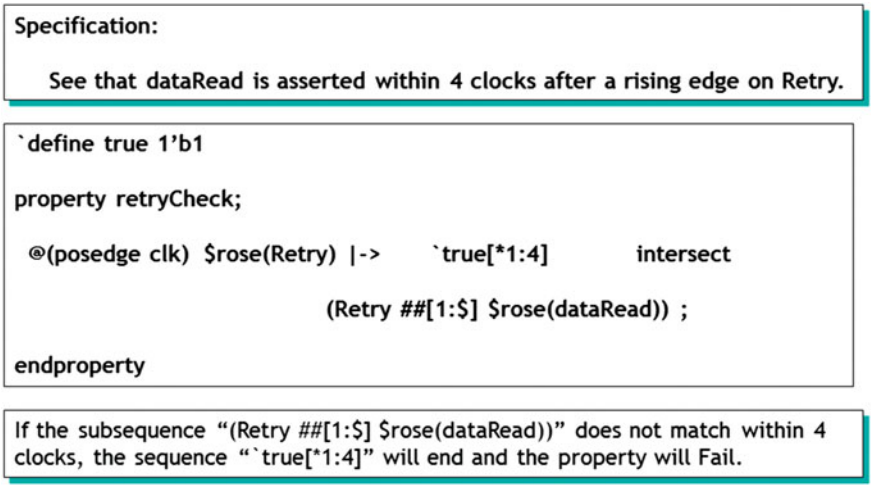


Fig. 6.47 Intersect operator: interesting application

If $rose(dataRead) does not arrive in 4 cycles the, the RHS will continue to execute beyond 4 clocks. But since 'true[*1:4] has now completed and since 'intersect' requires both sides to complete at the same time, the assertion will fail.

If $rose(dataRead) does occur within 4 clks, the property will PASS. Why? Please use the discussion above and you will be able to come up with an answer. I will leave it up to the reader to get the answer. Hint: 'true is with a range. *Any time* during the 'range' it is True.

So, what's the practical use of such a property. Any time you want to contain a large sequence to occur within a certain period, it is very easy to use the above technique. A large sequence may have many time domains and temporal complexities, but with the above method, you can simply superimpose 'true construct with 'intersect' to achieve the desired result.

6.14.2 'intersect' and 'and' :: What's the Difference?

See Fig. 6.48.

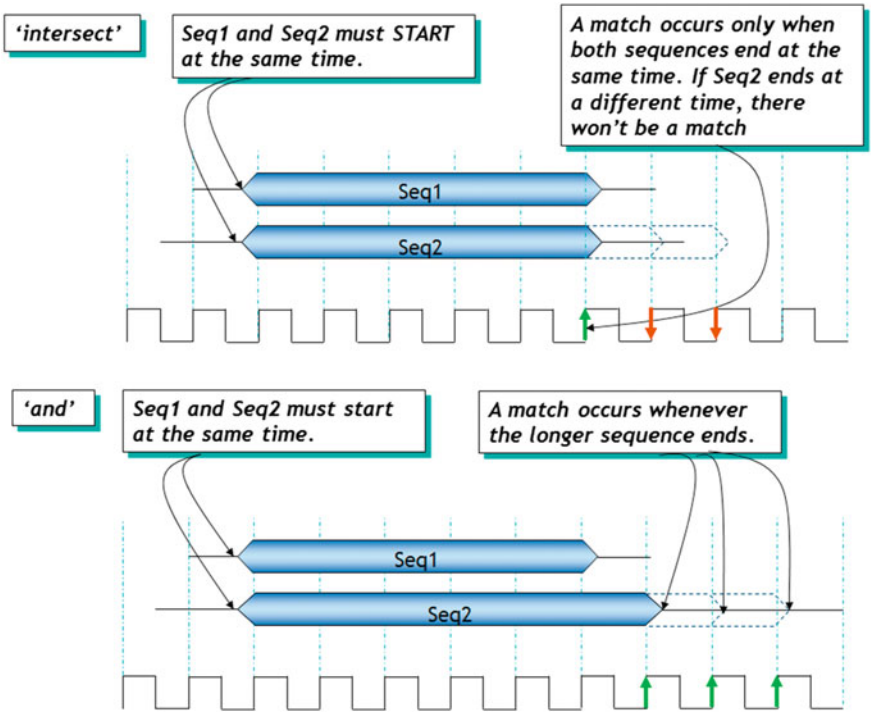


Fig. 6.48 *and* versus *intersect*—what is the difference

6.15 first_match

first_match(Seq)

- matches only the first of possibly multiple matches of the eval of Seq.
- useful for detecting the first occurance in a *delay range*.

6.15.1 Application: first_match

In Fig. 6.49, property 'fms' says that on the first_match of 'bcORef', 'a' should rise. As you notice, the sequence 'bcORef' has many matches because of the range operator and an 'or'. As soon as the first match of 'bcORef' is noticed, the property looks for $rose(a). In the top log, that is the case and the property passes. In the bottom log, $rose(a) does not occur and the property fails. The log middle is explained within the Fig. 6.49.

Figure 6.50 further explains 'first_match'. Annotations explain what's going on.

Figure 6.51 application clarifies $first_match further. This is the classic PCI bus protocol application. As the figure mentions, the first time frame_ && irdy_ are high (de-asserted) that the bus goes into IDLE state. Note that once frame_ and irdy_ are de-asserted the bus would remain in IDLE state for a long time. But we want the very first time that the bus transaction ends (indicated by frame_ && irdy_ high) that the bus goes into IDLE state. We do not want to evaluate any further busIdle conditions.

So, what would happen if you removed 'first_match' from the above property? The property will continue to look for state==busidle every clock that frame_ && irdy_ is high. Those will be totally redundant checks.

Note that in all the examples above, we have used first_match() in the antecedent. Why? Because *the consequent (RHS) of a property behaves exactly like first_match by definition*. The consequent is not evaluated once its first match is found (without the use of first_match). But the antecedent will keep firing every time there is a match of its expression.

Note the following 'cover' property. That further explains use of first_match.

abcProp: cover property (@ (posedge clk) a ##[1:4] b ##1 c);

Let us say, 'a' is true at time 10 and 'b' is true at time 20, thus meeting its requirement and then 'c' is true at time 30. The entire sequence matches and will be considered 'covered' (exercised). But if 'b' remains true at time 20,30,40 and 'c' remains true at 30,40,50, the coverage report will show multiple 'coverage' of this sequence. Something we do not really want. The following will solve the problem.

abcProp: cover property (@ (posedge clk) first_match (a ##[1:4] ##1 b ##1 c));

In this case, as soon as 'a' is true and 'b' is true the *first time* in ##[1:4] that 'c' is evaluated to be true the next clock and the property is considered covered. No further evaluation of this sequence will take place until 'a' is found asserted again.

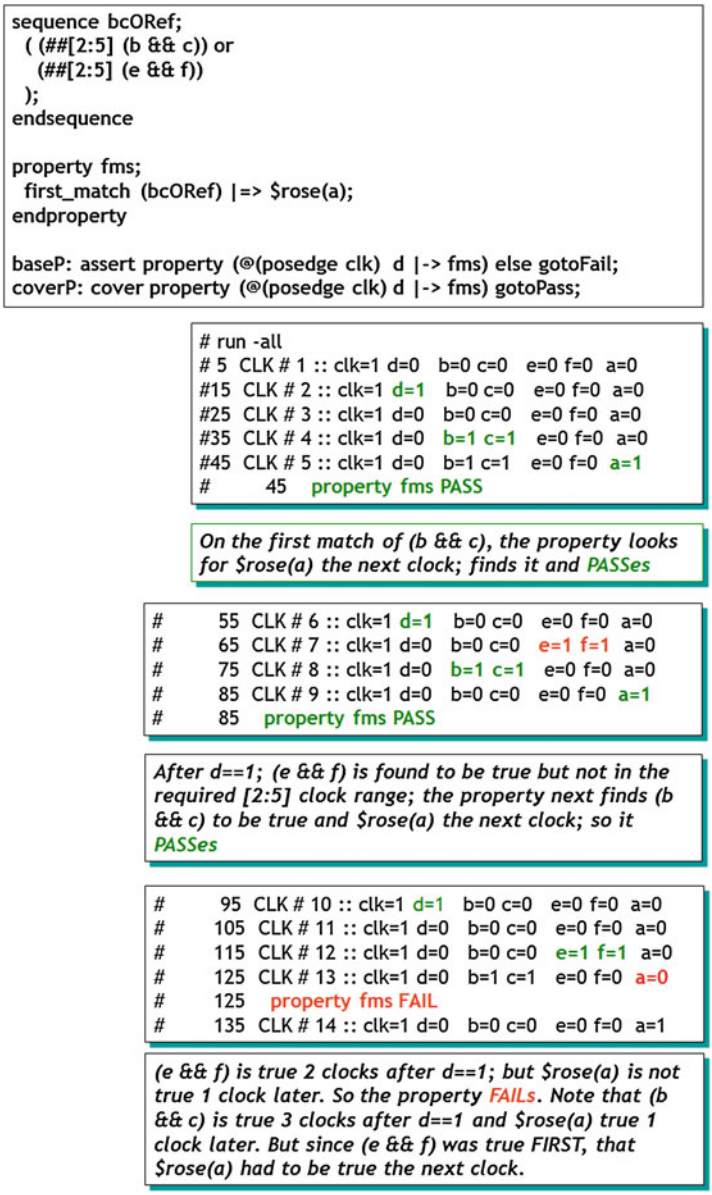


Fig. 6.49 first_match—application

In short, there can be many matches of a sequence but you want the evaluation to stop on the very first match that you use 'first_match'.

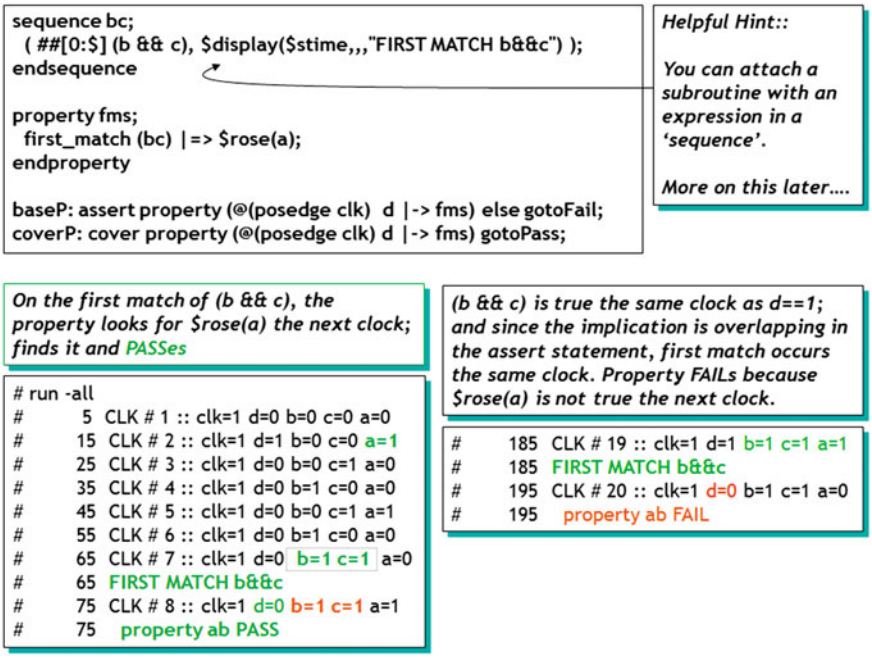


Fig. 6.50 *first_match* application

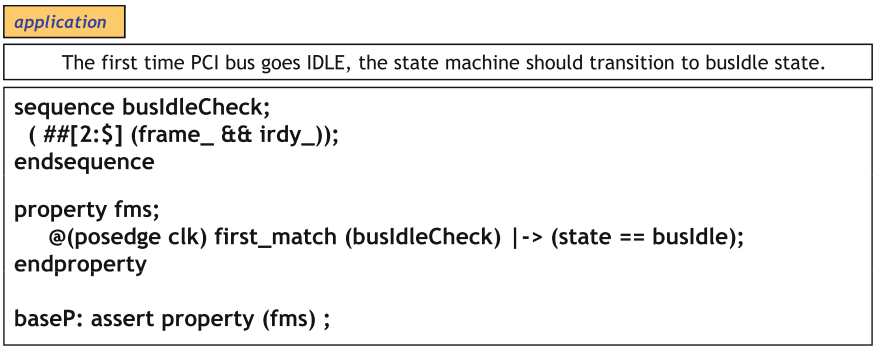


Fig. 6.51 first_match application

6.16 not <property expr>

The 'not' operator seems very benign. However, it could be easily misinterpreted because we are all wired to think positively—correct?

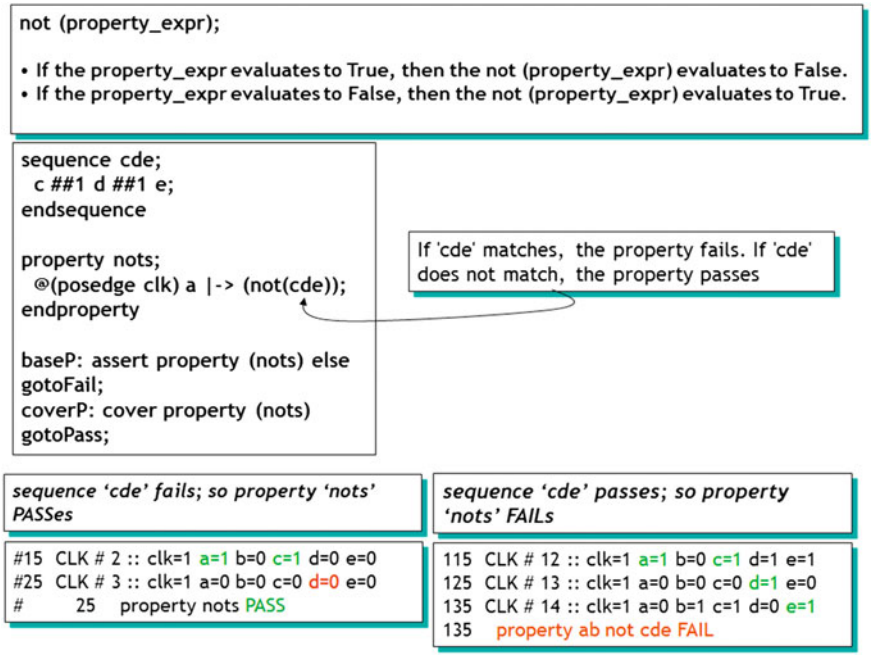


Fig. 6.52 not operator—basics

Figure 6.52 shows a use of 'not'. Whenever 'cde' is true the property will fail because of 'not' and pass if 'cde' is not true. Please refer to an example in Fig. 6.53 and then an application thereafter.

6.16.1 Application: not Operator

First, please refer to 'vacuous pass' in the Sect. 14.15 to understand the following application.

Figure 6.53 shows a classic mistake engineers make when using 'not' operator. Without the 'not' in this example if the antecedent "a ##1 b" does not match, the property vacuously passes (*vacuous pass is discussed in* ***section 14.5***) but nothing really happens. The property simply waits for the antecedent to be true so that the consequent can start its execution. However, since the antecedent has a 'not' in front of it, as soon as the property sees that the antecedent does not match it will fail (*not* of vacuous pass). That is indeed detrimental to your design results where many false failures would pop up.

As shown at the bottom of the figure, simply remove the implication operator "|->" and replace it with ##0, which has the same desired effect as the overlapping operator. However, since there is no implication operator, there is no vacuous pass.

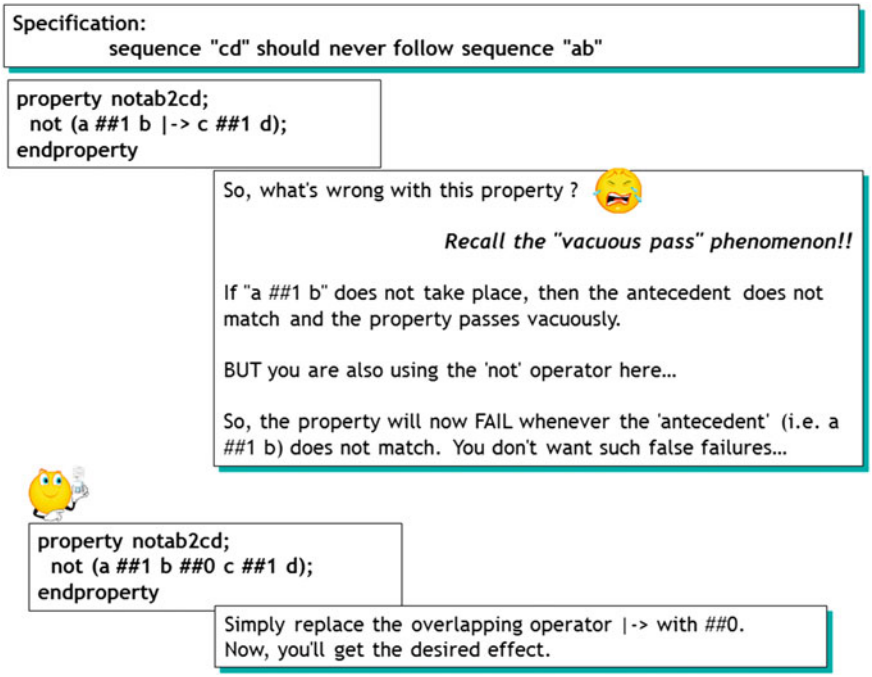


Fig. 6.53 not operator—application

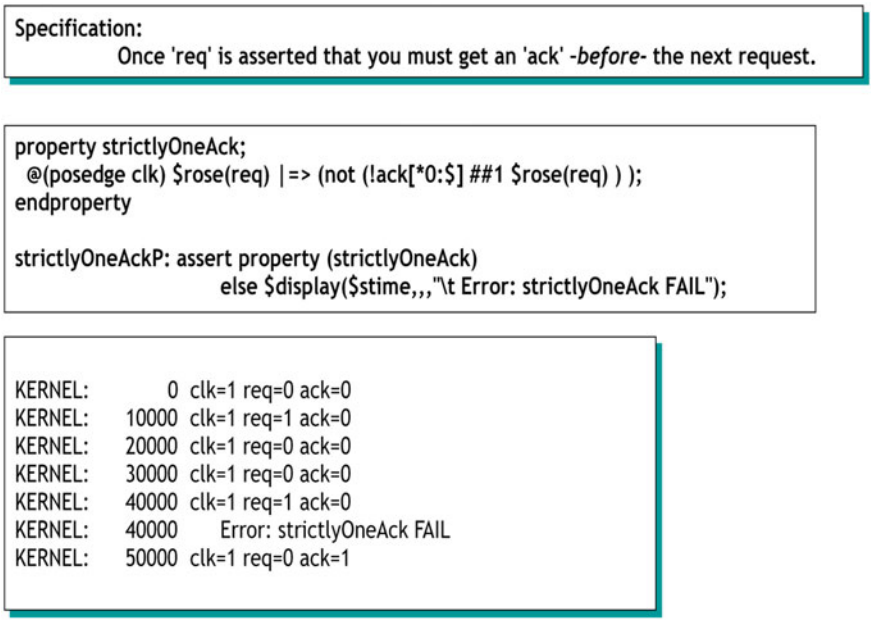


Fig. 6.54 *not* operator—application

Application in Fig. 6.54 is a very useful application. The specification says that once req is asserted (active high) that we must get an ack *before* getting another request. Such a situation occurs in many designs.

Let us examine the assertion. Property strictlyOneAck says that when 'req' is asserted (active high) that !ack[*0:$] remains low until $rose(req). If this matches than the property fails (because of the 'not').

In other words, we are checking to see that ack remains low until the next req, meaning if ack does go high before req arrives that the sequence (!ack[*0:$] ##1 $rose(req)) will fail and the 'not' of it will make it pass. That is the correct behavior since we *do* want an ack before the next req.

Or looking at it conversely (and as shown in the log), if 'ack' does remain low until the next 'req' arrives that the sequence (!ack[*0:$] ##1 $rose(req)) will pass and the 'not' of it will fail. This is correct also, because we do not want ack to remain low until next req arrives. We want 'ack' to arrive before the next 'req' arrives.

May seem a bit strange and this property can be written many different ways but this will give you a good understanding of how negative logic can be useful.

What is a simpler way to write this property?

6.17 if (expression) property_expr1 else property_expr2

```
if (expression) property_expr1;

OR

if (expression) property_expr1 else property_expr2;
```

```
property ife;
  @(posedge clk) a ##1 (b || c) [->1] |->
  if (b)
    (##1 d)
  else
    (##1 e);
endproperty

baseP: assert property (ife) else gotoFail;
coverP: cover property (ife) gotoPass;
```

```
The property reads as follows::

@(posedge clk) 'a' followed by at least
one 'b' OR 'c';

implies (|->)

that if 'b' is true than 1 clock later 'd' is
true else 1 clock later 'e' is true.
```

```
 5  CLK # 1 :: clk=1 a=0 b=0 c=0 d=0 e=0
15  CLK # 2 :: clk=1 a=1 b=0 c=0 d=0 e=0
25  CLK # 3 :: clk=1 a=0 b=0 c=0 d=0 e=0
35  CLK # 4 :: clk=1 a=0 b=1 c=0 d=0 e=0
45  CLK # 5 :: clk=1 a=0 b=0 c=0 d=1 e=0
45    property PASS
```

```
55  CLK # 6 :: clk=1 a=1 b=0 c=0 d=0 e=0
65  CLK # 7 :: clk=1 a=0 b=0 c=0 d=0 e=0
75  CLK # 8 :: clk=1 a=0 b=0 c=0 d=0 e=0
85  CLK # 9 :: clk=1 a=0 b=0 c=1 d=0 e=0
95  CLK # 10 :: clk=1 a=0 b=0 c=0 d=0 e=0
95    property FAIL
```

Fig. 6.55 *if… else*

'if' 'else' are similar to their counterpart in procedural language statements and obviously very useful. As the Fig. 6.55 annotates, we are making a decision in consequent based on what happens in the antecedent. The property 'if' states that on 'a' being true, either 'b' or 'c' should occur at least once, *any time* one clock after 'a'. If this antecedent is true, the consequent executes. Consequent expects 'd' to be true if 'b' is true and 'e' to be true if 'b' is false or 'c' is true.

The simulation log in the bottom left of Fig. 6.55 shows that at time 15, 'a==1' and 1 clock later 'b' is true as required. Since 'b' is true, 'd' is true 1 clock later at time 45. Everything works as required and the property passes. In the bottom right simulation log, 'a==1' at time 55 and 'c' goes true at 85. This would require 'e' to be true 1 clock later, but it is not and the property fails. This is just but one way to use if-else and tie in antecedent with consequent.

Based on the analogy of the Fig. 6.55, a practical application is given in Fig. 6.56.

6.17.1 Application: if then else

Specification :

On a TagCompare,

if there is a TagHit, start mesiCompare
else start an allocRead

application

```
property tagCheck;
  @(posedge clk) (State == TagCompare) ##1 (TagHit || TagMiss) |->

  if (TagHit)
    ##1 (State == mesiCompare)

  else
    ##1 (State == allocRead);

endproperty

baseP: assert property (tagCheck) else gotoFail;
coverP: cover property (tagCheck) gotoPass;
```

Fig. 6.56 if… else—application

This property is self-explaining. On a TagCompare, if it is a hit, start MESI compare else start a Read Allocation cycle.

Chapter 7
System Functions and Tasks

7.1 $onehot, $onehot0

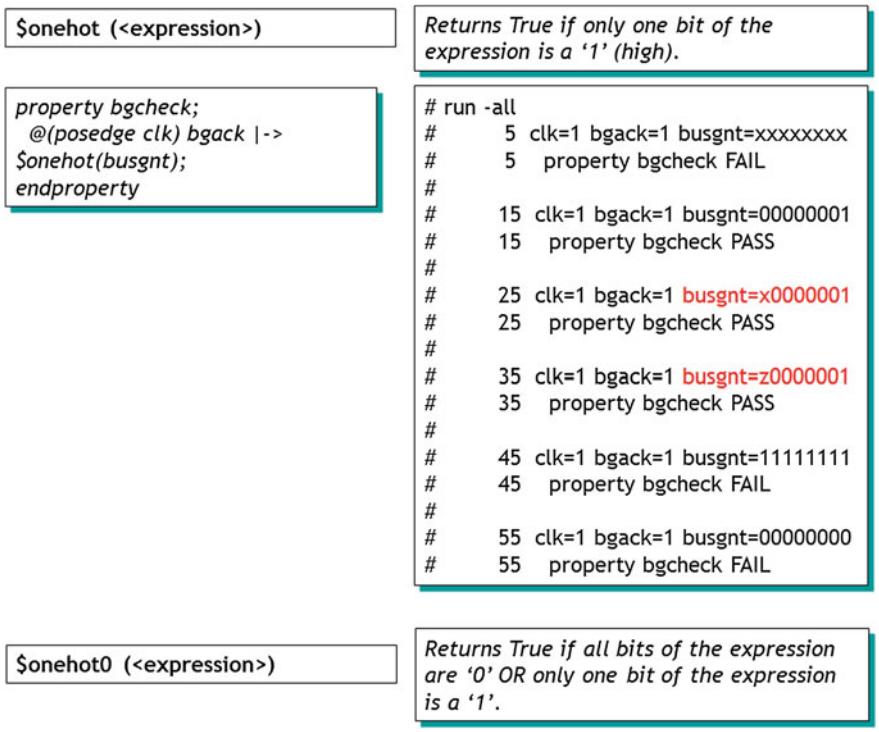


Fig. 7.1 $onehot and $onehot0

A. B. Mehta, *SystemVerilog Assertions and Functional Coverage*,
DOI: 10.1007/978-1-4614-7324-4_7,

$onehot and $onehot0 are quite self explanatory and are explained in the Fig. 7.1. *Note that if the expression is 'Z' or 'X' that $onehot or $onehot0 will fail.*

A simple application is described in the Fig. 7.1. For any acknowledge of a bus grant there can be only one bus grant. This is very easily accomplished by $onehot as shown.

7.2 $isunknown

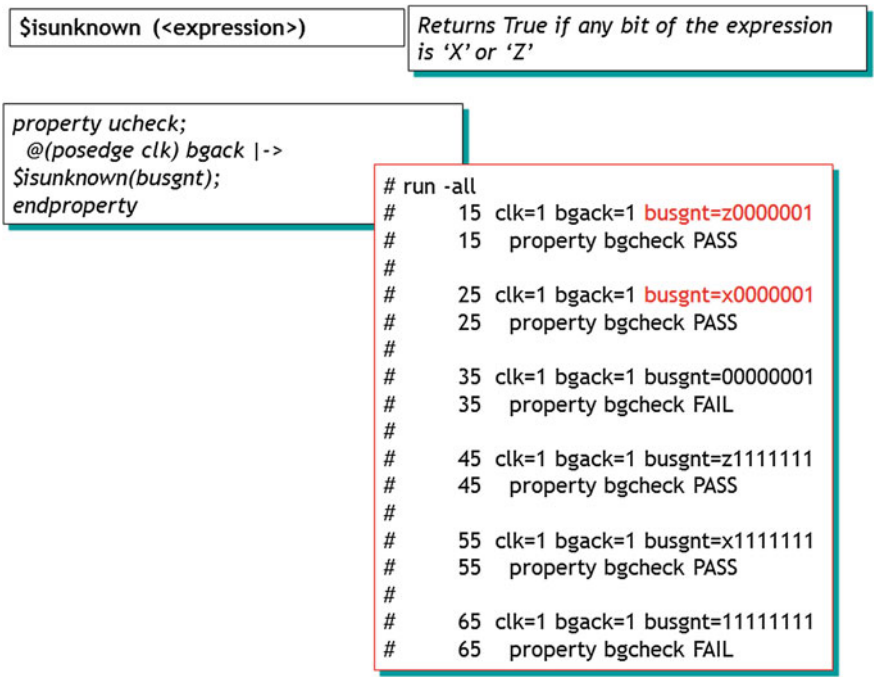


Fig. 7.2 $isunknown

$isunknown passes if the expression is unknown ('X' or 'Z'). In other words, if the expression is not unknown then the property will fail! *Hence, if you do want a failure on detection of an unknown ('X' or 'Z') then you have to negate the result of $isunknown*. Simple but easy to miss.

Simulation log in Fig. 7.2 clarifies the concept. Property 'ucheck' states that if 'bgack' is true that the 'busgnt' is unknown. What? This is simply to show what happens if you use $isunknown without a 'not'.

7.2.1 Application $isunknown

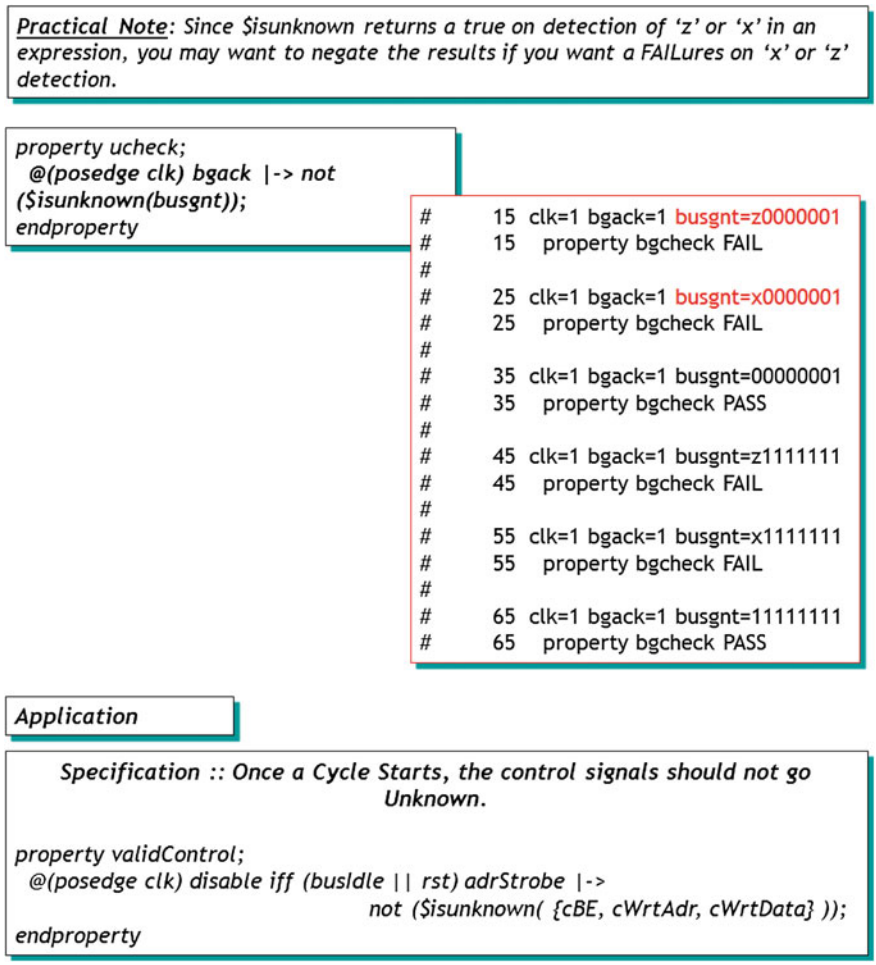


Fig. 7.3 $isunknown application

Figure 7.3 shows two simple applications. First is identical to the one we just discussed, but with a 'not'.

@(posedge clk) bgack |-> not ($isunknown(busgnt));

It says, if bgack is true (high) that busgnt must not be in unknown state. Again, note that $isunknown returns a true on detection of an unknown. So, if you want a failure, you have to negate the result. This is shown in the simulation log above. The second application (bottom of Fig. 7.3), says that if 'adrStrobe' is High that the control signals cannot be unknown.

7.3 $countones

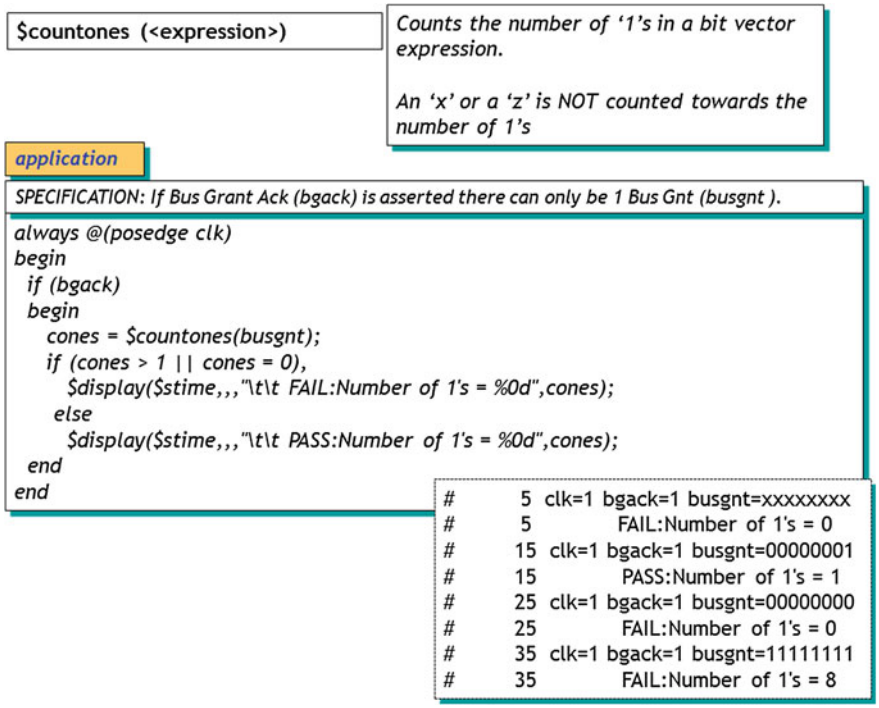


Fig. 7.4 $countones—basics and application

$countones is very simple but powerful feature. Note that the system function can be used in a procedural block as well as in a concurrent property/assertion.

Figure 7.4 shows an application which states that if there is a bus grant acknowledge (bgack) that there can be only 1 bus grant (busgnt) active on the bus. Note that we are using $countones in a procedural block in this example. Note also that if the entire 'busgnt' is unknown ('X') or tri-state ('Z'), the assertion will fail. Figure 7.5 shows a very simple way to check for Gray Code compliancy.

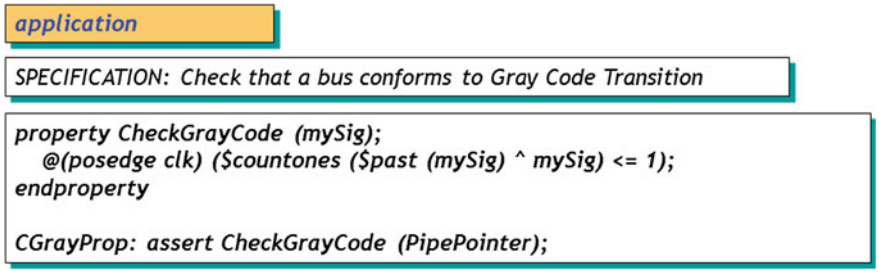


Fig. 7.5 $countones application

7.3.1 $countones (as a boolean)

$countones returns the # of 1's in an expression. It can also be used to determine 'true'ness of the expressions.

In other words, it can be used for pass/fail indication.

If there is at least One '1', it's a pass, else it's a fail

```
property bgcheck;
  @(posedge clk) bgack |-> $countones(busgnt);
endproperty
```

```
#       15  clk=1 bgack=1 busgnt=00000001
#       15    property bgcheck PASS
#
#       25  clk=1 bgack=1 busgnt=00000000
#       25    property bgcheck FAIL
#
#       35  clk=1 bgack=1 busgnt=000000x1
#       35    property bgcheck PASS
#
#       45  clk=1 bgack=1 busgnt=000000z1
#       45    property bgcheck PASS
```

Fig. 7.6 $countones as boolean

7.4 $assertoff, $asserton, $assertkill

There are many situations when you want to have a global control over assertions both at module and instance level. Recall that 'disable iff' provides you a local control directly at the source of the assertion.

As noted in Fig. 7.7, **$assertoff** temporarily turns off execution of all assertions. Note that if an assertion is under way when **$assertoff** is executed, the assertion would not be killed. You restart assertion execution on a subsequent invoke of $asserton. **$assertkill** will kill *all* assertions in your design *including* already executing assertion. And it would not automatically start when the next assertion starts executing. It will start executing only on the subsequent $asserton. $**asserton**: This is the default. It is required to restart assertions after a $assertoff or $assertkill.

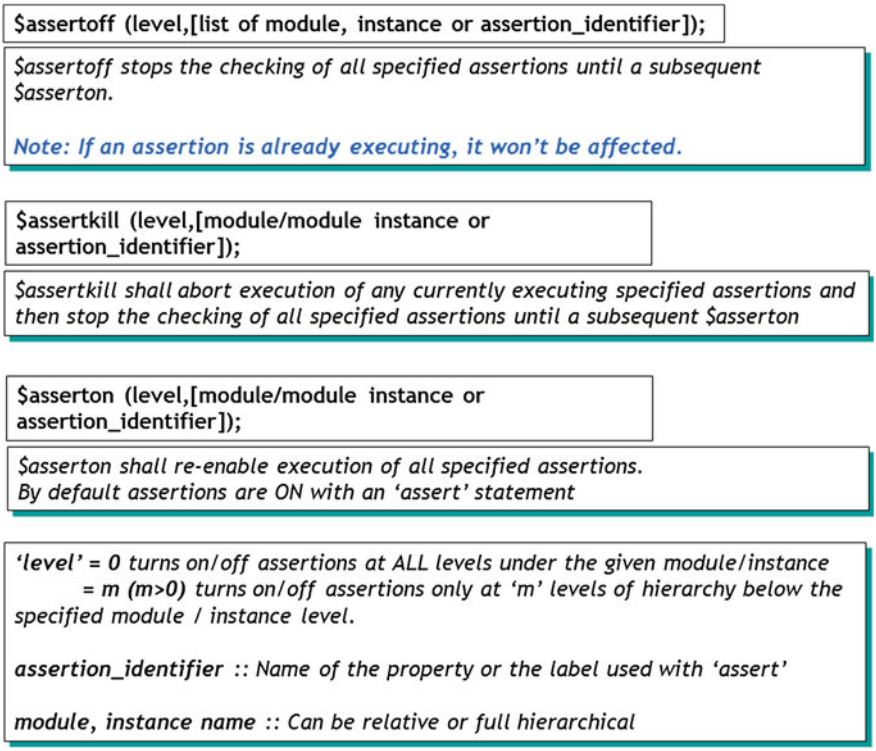


Fig. 7.7 $assertoff, $asserton, $assertkill—Basics

Following is a typical application deployed by projects to suppress execution of assertions during reset or during an exception, if so required (Fig. 7.8).

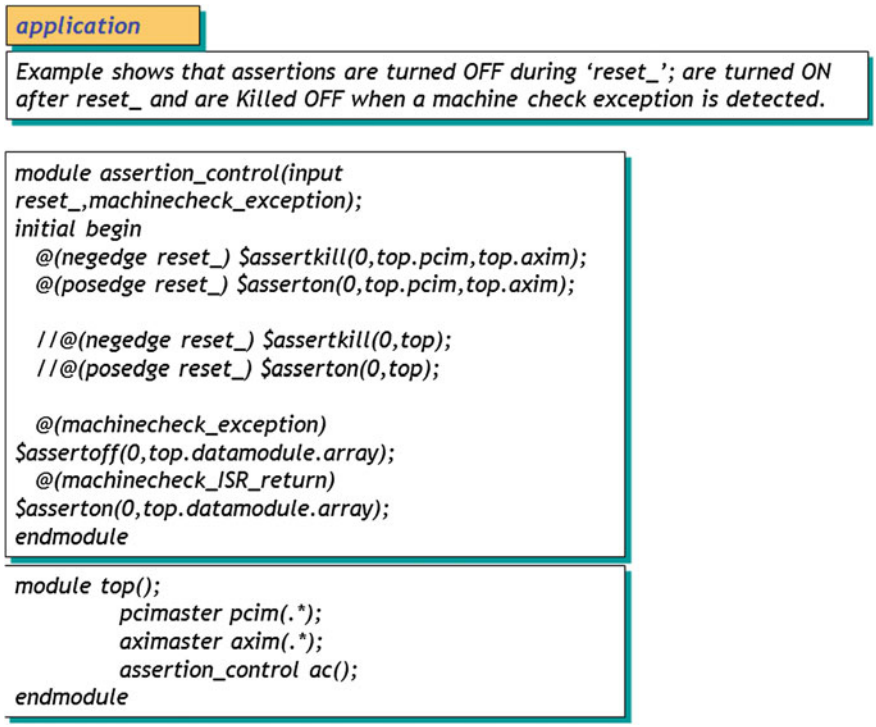


Fig. 7.8 Assert control application

Chapter 8
Multiple Clocks

8.1 Multiply Clocked Sequences and Property Operators

There are hardly any designs anymore that work only on a single clock domain. So far we have seen properties that work off of a single clock. But what if you need to check for a temporal domain condition that crosses clock boundaries. The so-called CDC (clock domain crossing) issues can be addressed by multiple clock assertions.

We'll thoroughly examine how a property/sequence crosses clock boundary. What's the relationship between these 2 clocks? How are sampling edges evaluated once you cross the clock domain. Note that in a singly clocked system, the sampling edge is always one—that is the clock posedge or negedge. Since there are two (or more) clocks in multiply clocked system, we need to understand how the sampling edges cross boundary from one clock to another. I think it is best to fully understand the fundamentals before jumping into applications.

Note that there are differences in the way a 'sequence' behaves for multiple clocks and the way a property behaves. Read on…

Figure 8.1 shows a simple multiply clocked sequence. It says at (posedge clk0) A is true and the *very next nearest strictly subsequent* (posedge clk1) B is true. Note the emphasis on 'very next'. That is because when you join two subsequences each of which runs on a different clock, you can only transition from one clock domain to the next clock domain's very next available sampling edge. This will be clearer when we dive a bit more into detail.

Jumping ahead a bit, this '*very next nearest strictly subsequent edge*' semantic is why we use ##1 to cross clock boundaries. So, can you use ##2 when crossing clock boundaries? Keep this question in mind as you learn basics of multiply clocked sequences and properties.

A. B. Mehta, *SystemVerilog Assertions and Functional Coverage*,
DOI: 10.1007/978-1-4614-7324-4_8,

8.1.1 Multiply Clocked Sequences

The timing diagram in Fig. 8.1 shows that at (posedge clk0), 'A' is true. The clocks are out of phase, so the very next clock edge of clk1 is half a clock delayed from posedge clk0. At the posedge clk1 'B' is sampled true and the sequence 'mcloks' will pass. The point here is that '##1 @ (posedge clk1)' waited only for ½ clk1 and not a full cycle because the *very next nearest strictly subsequent posedge clk1* arrived within ½ clock period. The next clock can come in any time after clock0 and that will be the 'very next' edge taken as the sampling edge for that subsequence.

Important Note:
The requirement of ##1 between two subsequences have been removed from 1800 to 2009. I am leaving it here for those who are using 1800-2005 and have not yet moved to 1800-2009.

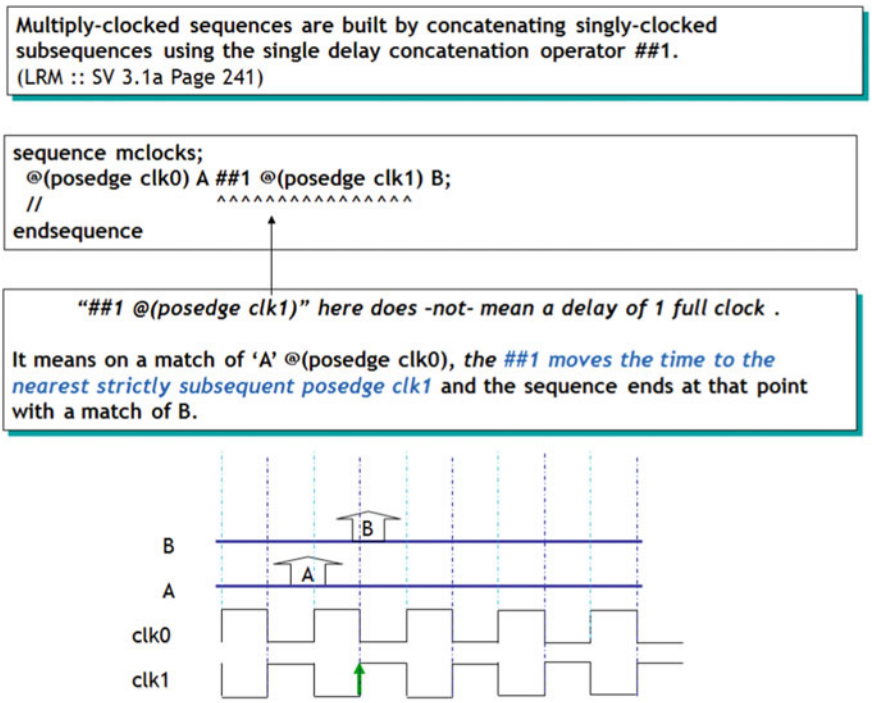


Fig. 8.1 Multiply clocked sequences—basics

So, what happens if clk0 and clk1 are in phase? See Fig. 8.2 below. The explanation is in the figure itself. As self-evident, the sequence will wait for

one full clk before sampling 'B'. But more importantly note that, if the clocks on the clock crossing boundary are identical (in phase and same period), then the following is true.

@ (posedge **clk0**) A ##1 @ (posedge **clk1**) B; *is identical to*
@ (posedge **clk0**) A ##1 @ (posedge **clk0**) B; *is identical to*
@ (posedge **clk0**) A ##1 B;

To reiterate the earlier concept, the above are identical because ##1 @ (posedge xxx) does not mean 2 clock edges. It simply means the very next subsequent edge of the next clk.

```
//ASSUME clk0 is identical to clk1

sequence mclocks;
  @(posedge clk0) A ##1 @(posedge clk1) B;
          //(Or @(posedge clk0) A ##1 @(posedge clk0) B; )
endsequence
```

If both clocks are identical then the clocking event does not change after the ##1 delay and the above sequence is equivalent to

```
@(posedge clk0) A ##1 B;
```

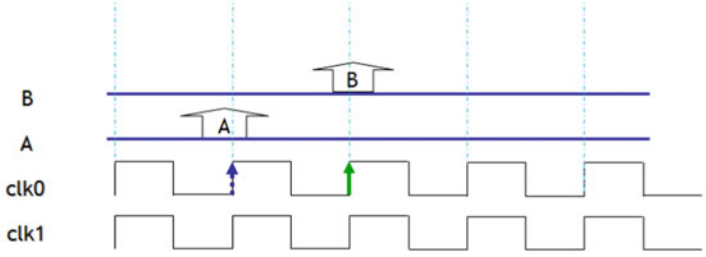


Fig. 8.2 Multiply clocked sequences—identical clocks

8.1.2 Multiply Clocked Sequences: Legal and Illegal Sequences

Before we move onto multiply clocked properties and based on our observations, let us quickly examine the legal and illegal cases of multiply clocked sequences. *Again, these cases apply only to sequences and not properties.*

Bottom line is that you can only have ##1 between two subsequences with different clocks. If the clocks are the same on both sides then there is not such restriction. Figure 8.3 makes it clear.

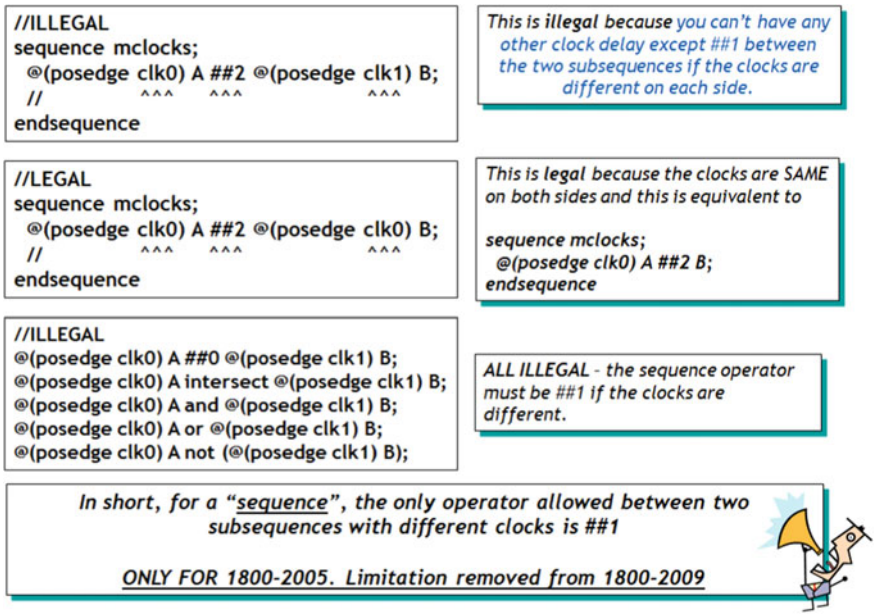


Fig. 8.3 Multiply clocked sequences—illegal conditions—ONLY FOR 1800-2005. Limitation removed from 1800-2009

Note To reiterate, the above restriction is true only for IEEE 1800-2005 standard. This restriction has been removed from 1800-2009. I am still describing the restriction here, in case you are using 1800-2005 and have not yet moved to 1800-2009.

8.1.3 Multiply Clocked Properties—'and' Operator

The concept of 'and' of two sequences has been discussed before. But what if the clocks in the sequences are different? The important thing to note above is the concept of the very next strictly subsequent edge. In Fig. 8.4, at the posedge of clk0, 'a' is sampled high. That triggers the consequent that is an 'and' of 'b' and 'c'. Note that 'b' is expected to be true at the very next edge of clk1 (after the posedge of clk0). *In other words, even though there is a non-overlapping operator in the property, we don't quite wait for 1 clock*. We simply wait for the very next posedge of clk1 to check for 'b' to be true. The same story applies to 'c'. When both 'b' and 'c' occur as shown in Fig. 8.4, the property will pass. As with the singly clocked 'and', the assertion passes at the match of the longest (so to say) sequence 'c'.

```
property mclocks;
  @(posedge clk1) b and @(posedge clk2) c;
endproperty

baseP: assert property (@(posedge clk0) a |=> mclocks) else
gotoFail;
coverP: cover property (@(posedge clk0) a |=> mclocks) gotoPass;
```

'B' and 'C' must be true at immediate next posedge of clk1 and clk2 respectively after the posedge of clk0

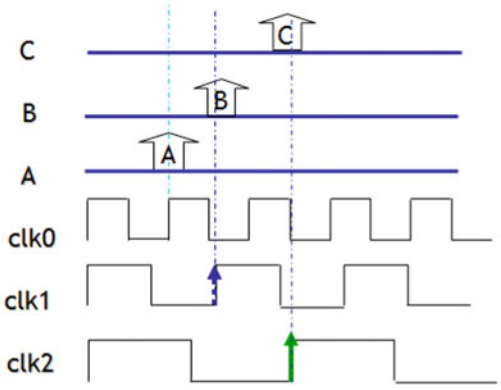


Fig. 8.4 Multiply clocked properties—'and' operator between two different clocks

Figure 8.5 shows another scenario to solidify the concept of 'and' for multiply clocked assertions. The 'and' is between two subsequences which use the same clock. The behavior is obvious but interesting. This is because "@ (posedge clk1) b and @ (posedge clk1) c" acts essentially like "@ (posedge clk1) b **and** c". Hence, both the 'b' and the 'c' must now occur at the very next posedge of clk1.

In short, as we saw before, "@ (posedge clk1) b **and** @ (posedge clk1) c" is identical to "@ (posedge clk1) b **and** c".

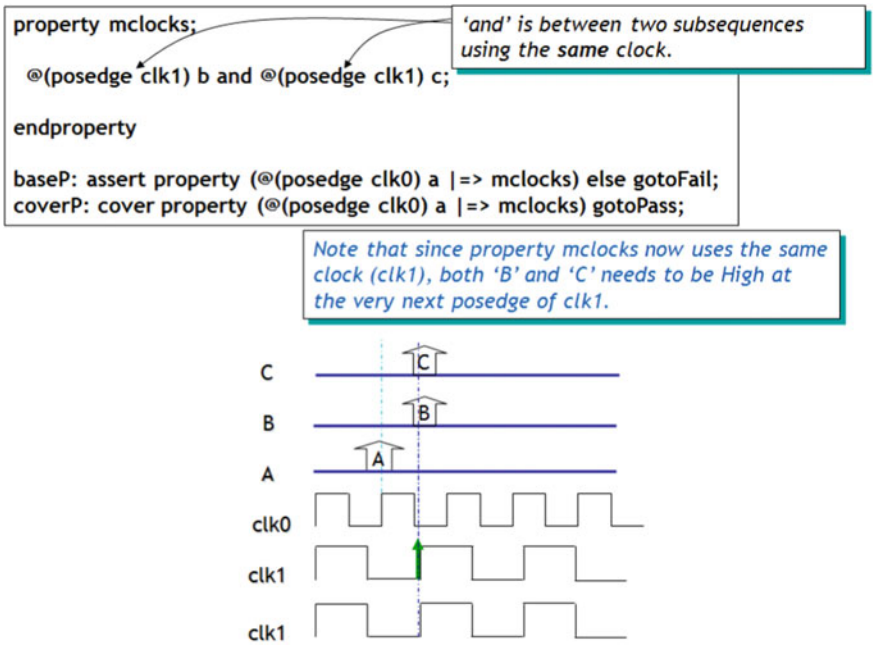


Fig. 8.5 Multiply clocked properties—'and' operator between same clocks

8.1.4 Multiply Clocked Properties—'or' Operator

All the rules of 'and' apply to 'or'—except as in singly clocked properties—when either of the sequence (i.e. either the LHS or RHS of the operator) passes that the assertion will pass. The concept of 'the very next strictly subsequent clock edge' is the same as with 'and'.

Please refer to Fig. 8.6 for better understanding of 'or' of multiply clocked sequences. The property passes when either @ (posedge clk1) b or @ (posedge clk2) c occurs. In other words, if @ (posedge clk2) c occurs before @ (posedge clk1) b, the property will pass at @ (posedge clk2) c.

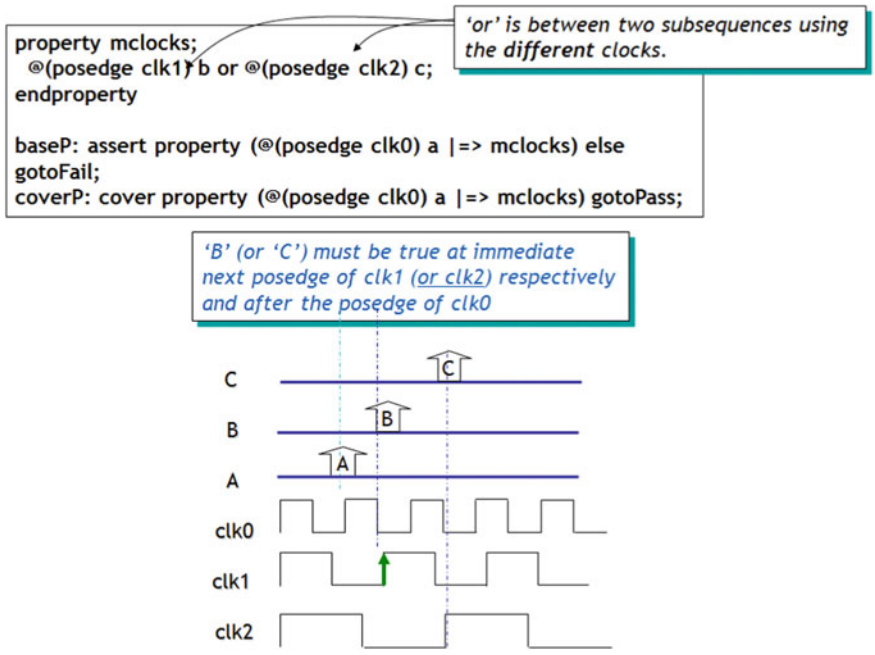


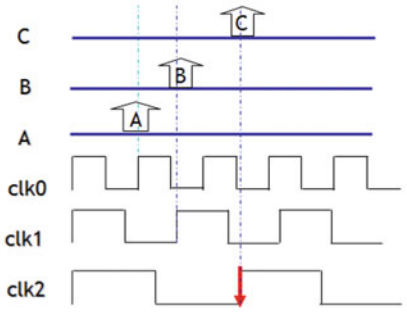
Fig. 8.6 Multiply clocked properties—'or' operator

8.1.5 Multiply Clocked Properties—'not' Operator

'not' is an interesting operator when it comes to multiply clocked assertions.

The assertion in Fig. 8.7 below works as follows. At posedge clk0, 'a' is true which triggers the consequent mclocks. The property mclocks specifies that @ posedge clk1 'b' needs to be true and 'c' should –not- be true @ posedge clk2. The timing diagram shows that 'a' is true at posedge clk0. At the subsequent edge of clk1 'b' should be true and since it is indeed true, the property moves along. Because of an 'and' it looks for 'c' to be true at the next (in other words, the very first subsequent posedge clk2 after the posedge of clk0) edge of clk2. Well, 'c' is indeed true but since we have a 'not' in front of @ (posedge clk2), the property will fail. The concept of 'not' is the same as that of singly clocked properties except for the edge of the clock when it is evaluated. The simulation log clarifies the concept.

```
property mclocks;
  @(posedge clk1) b and (not (@(posedge clk2) c) );
endproperty

baseP: assert property (@(posedge clk0) a |=> mclocks) else
gotoFail;
coverP: cover property (@(posedge clk0) a |=> mclocks) gotoPass;
```




```
# run -all

#        0  clk0,1,2=111 a=0 b=0 c=0
#       10  clk0,1,2=101 a=1 b=0 c=0
#       16  clk0,1,2=010 a=1 b=1 c=0
#       20  clk0,1,2=110 a=1 b=1 c=0
#       24  clk0,1,2=101 a=1 b=1 c=1
#       24    property mclocks FAIL

#       30  clk0,1,2=101 a=1 b=1 c=0
#       32  clk0,1,2=111 a=1 b=1 c=0
#       40  clk0,1,2=100 a=0 b=0 c=0
#       48  clk0,1,2=011 a=1 b=1 c=0
#       48    property mclocks PASS
```

Fig. 8.7 Multiply clocked properties—'not' operator

8.1.6 Multiply Clocked Properties—Clock Resolution

```
property mclocks;
  @(posedge clk0) A |->
          if (D) @(posedge clk0) B;
endproperty
```

This is equivalent to
@(posedge clk0) A |-> if (D) B;

```
property mclocks;
  @(posedge clk0) A |->
          if (D) @(posedge clk0) B
          else @(posedge clk0) (!B);
endproperty
```

This is equivalent to
@(posedge clk0) A |-> if (D) B else (!B) ;

```
property mclocks;
  @(posedge clk0) A |->
          if (D) @(posedge clk0) B
          ##1 @(posedge clk1) Z
          else @(posedge clk0) (!B);
endproperty
```

This is equivalent to
@(posedge clk0) A |-> if (D) B ##1
@(posedge clk1) Z else (!B) ;

```
property mclocks;
  @(posedge clk0) A |->
          if (D) @(posedge clk0) B
          else @(posedge clk1) (!B);
endproperty
```

ILLEGAL
Cannot have two different clocks on two sides of the overlapping operator (|->). You need a non-overlapping operator (|=>) for this to work.

Fig. 8.8 Multiply clocked properties—clock resolution

These rules are important to follow when you are dealing with multiply clocked properties. The important rule to note is the ILLEGAL rule. *You cannot use an overlapping operator when the clocks are different in the antecedent and consequent*. For the clocks to be different, you must use a non-overlapping implication operator (Fig. 8.8).

Figures 8.9 and 8.10 illustrate other important concepts. How do clocks apply (or flow) from one part of sequence to another? The description in the figure explains how this works.

1. In Fig. 8.9, property 'mclocks' (posedge clk0) applies to 'A' as well as 'B' since 'B' does not have an explicit clock. So far so good.
2. Then (posedge clk1) applies to 'C'. That also makes sense.
3. But what clock is applied to 'D' in the consequent since 'D' does not have its own explicit clock?
4. According to the 1800-2005 LRM, 'D' will inherit (posedge clk0) and *not* the (posedge clk1). This is not quite intuitive. But LRM makes it very clear that "the scope of a clocking event does not flow out of enclosing parenthesis".
5. In our case ('B' ##1 @ (posedge clk1) C) is in parenthesis. So once we are out of that parenthesis (posedge clk1) does not flow forward but (posedge clk0) moves forward to the consequent 'D'.

```
property mclocks;
 @(posedge clk0) A ##1 (b ##1 @(posedge clk1) C) |=> D;

endproperty
```

```
Here clk0 flows through 'A' then in the parenthesis to 'B' but not through 'C';
But once out of the parenthesis, it then flows through 'D'

 //LRM: System Verilog 3.1a, Page 244:
 //"The scope of a clocking event flows into parenthesized sub expressions and, if
 //the sub expression is a sequence, also flows left-to-right across the parenthesized
 //sub expression. However, the scope of a clocking event does not flow out of
 //enclosing parenthesis".
```

```
sequence s1;
 @(posedge clk0) b ##1 c;
endsequence

sequence s2;
 @(posedge clk1) d ##1 e;
endsequence

sequence s;
 @(posedge clk) a ##1 s1 ##1 s2 ##1 f;

endsequence
```

Fig. 8.9 Multiply clocked properties—clock resolution—II

Similarly, the bottom example in Fig. 8.9 shows how the clock would 'flow' when we have multiple subsequences each with its own clock. Note that there are three different clocks in this sequence. (posedge clk) flows through 'a'. Then 's1' and 's2' use their own clocks as sampling edges (clocks) for their sequences. But once out of 's2', (posedge clk) is applied to 'f' –not- the (posedge clk1) of 's2'.

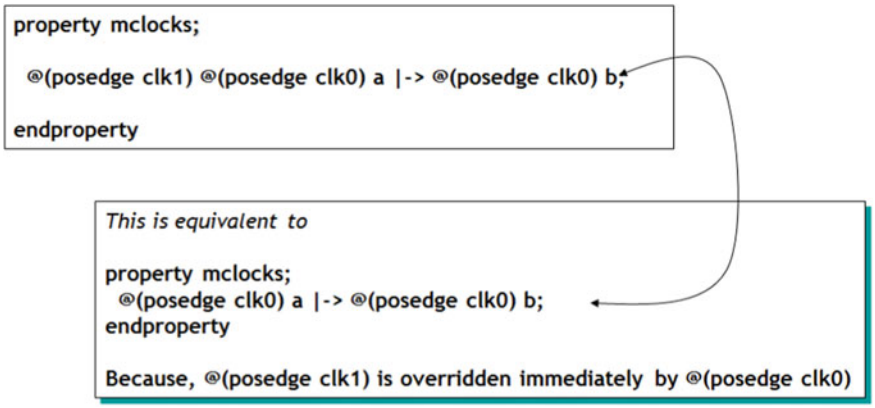


Fig. 8.10 Multiply clocked properties—clock resolution—III

Figure 8.10 shows another interesting property. What will happen if you need to transition from one clock to another before checking for an expression/sequence? Well, you cannot quite do that. In Fig. 8.10, we show that (posedge clk1) is immediately followed by (posedge clk0). This does *not* mean that the property will wait first for (posedge clk1) then for (posedge clk0) and then apply (posedge clk0) to 'a'. It will simply override (posedge clk1) with (posedge clk0) and directly apply (posedge clk0) to 'a'. This is shown in the bottom of the figure in the equivalent property.

8.1.7 Multiply Clocked Properties—Legal and Illegal Conditions

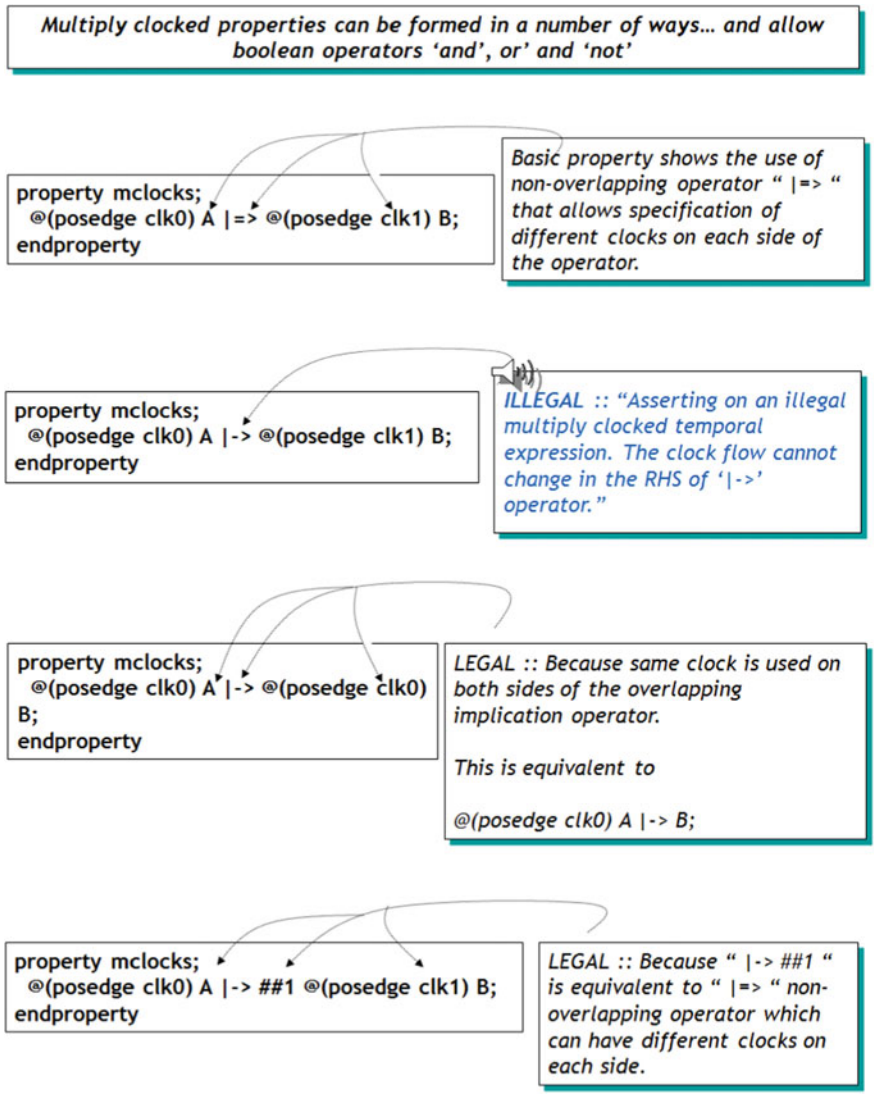


Fig. 8.11 Multiply clocked properties—legal and illegal conditions

Figure 8.11 is a recap as an easy reference to legal and illegal semantics of multiply clocked properties.

The top most example shows that it's ok to have different clocks between the antecedent and the consequent, as long as the implication operator is non-overlapping.

The second example shows that this would be illegal if the clocks on both sides of the implication operator were different and the implication operator was overlapping.

But as shown in the third example, overlapping operator is perfectly legal if the clocks on both sides of the overlapping operator are the same.

And the last example is quite intuitive in that "=>"is equivalent to "| ->##1". Hence, you can have different clocks on each side of overlapping operator.

Chapter 9
Local Variables

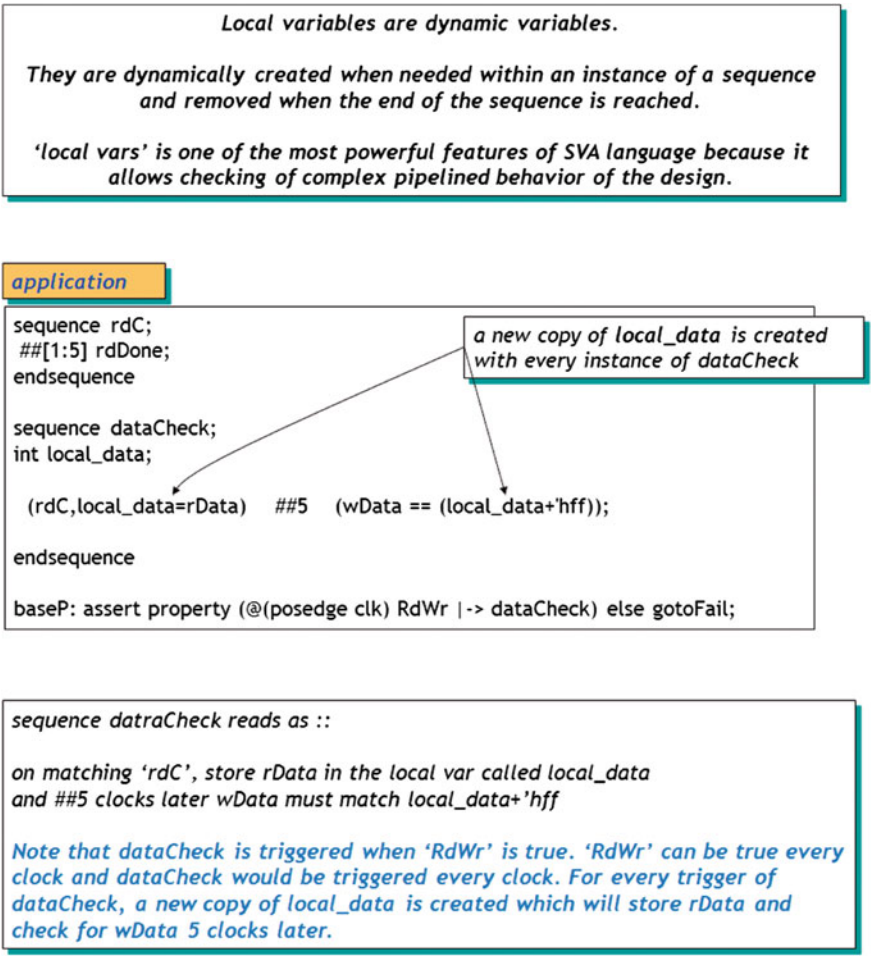


Fig. 9.1 Local variables—basics

A. B. Mehta, *SystemVerilog Assertions and Functional Coverage*,
DOI: 10.1007/978-1-4614-7324-4_9,

Local variable is a feature you are likely to use very often. They can be used in both a sequence and a property. They are called local because they are indeed local to a sequence and are not visible or available to other sequences or properties. Of course, there is a solution to this restriction, which we will study further into the section. Figure 9.1 points out key elements of a local var. The most important and useful aspect of a local variable is that it *allows multi-threaded application and creates a new copy of the local variable with every instance of the sequence in which it is used*. User does not need to worry about creating copies of local variables with each invocation of the sequence. Above application says that whenever 'RdWr' is sampled high at a posedge clk, that 'rData' is compared with 'wData' 5

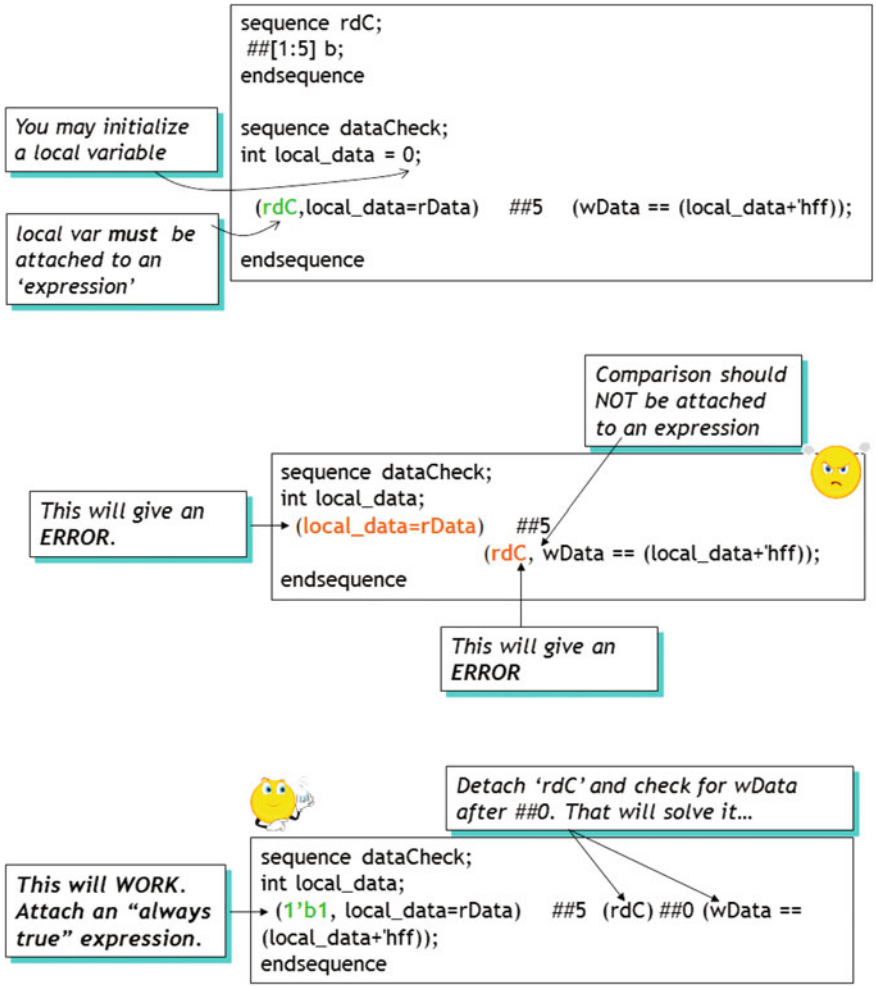


Fig. 9.2 Local variables—Do's and Don'ts

clocks later. The example shows how to accomplish this specification. Local variable 'int local_data' stores the 'rData' at posedge of clk and then compares it with wData 5 clocks later. Note that 'RdWr' can be sampled true at every posedge clk. Sequence 'data_check' will enter every clock; create a new copy of local_data and create a new pipelined thread that will check for local_data+'hff with 'wData' 5 clocks later. Moving along, Fig. 9.2 shows other semantics of local variables. *Pay close attention to the rule that local variable must be 'attached' to an expression while comparison cannot be attached to an expression*!!

As shown in Fig. 9.2, *a local variable must be attached to an expression when you store a value into it. But when you compare the value stored in a local variable, it must not be attached to an expression.*

In the topmost example, "local_data=rData) is attached to the sequence 'rdC'. In other words, assignment "local_data=rData" will take place only on completion of sequence 'rdC'. Continuing with this story of storing a value into a local variable, what if you don't have anything to attach to the local variable when you are storing a value? Use 1'b1 (always true) as an expression. That will mean whenever you enter a sequence, that the expression is always true and you should store the value in the local variable. Simple!

Similarly, what if you compare a value on an expression being true? As shown in Fig. 9.2, you can indeed accomplish this by 'detaching' the expression as shown. The resulting sequence (the last sequence in the Fig. 9.2) will read as "on entering dataCheck, store rData into local_data, wait for 5 clocks and then if 'b' (of sequence rdC) is true within 5 clocks, compare wData with stored local_data + 'hff".

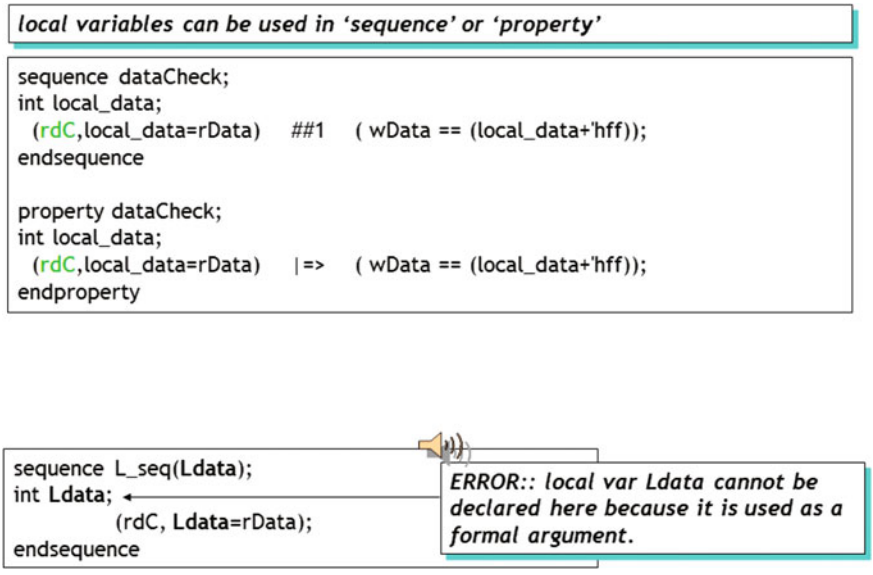


Fig. 9.3 Local variables—and formal argument

Figure 9.3 points out a couple of other important features. First, there is no restriction in using a local variable in either a sequence or a property. In addition, you cannot declare a local variable as a formal and pass as an actual from another sequence/property. That makes sense, else why would it be called 'local'?

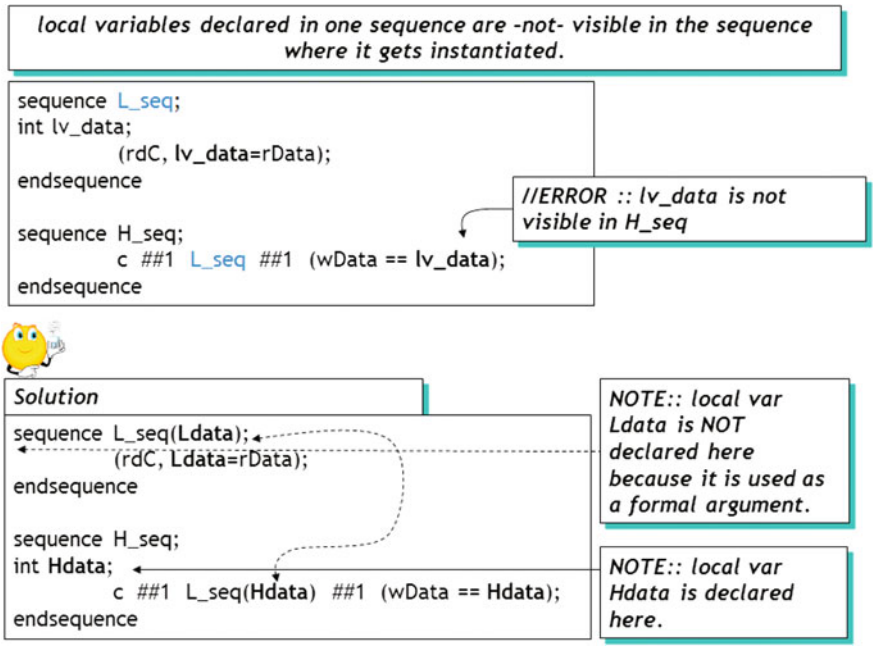


Fig. 9.4 Local variables—visibility

In Fig. 9.4, we see that a local variable in a sequence is not visible to the sequence that instantiates it. The solution is quite straightforward. Instead of poking at the local variable directly, simply pass an argument to the sequence that contains the local variable. When the sequence L_seq updates the argument locally, it will be visible to the calling sequence (H_seq). Note that Ldata is not declared as a local variable in sequence L_seq (else that would be an error as we discussed). L_seq simply updates a formal and passes it to the calling sequence, where the actual is declared as a local variable. This is shown in the bottom of Figs 9.4, 9.5.

Figures 9.6, 9.7, 9.8, 9.9, 9.10, 9.11, 9.12 shows finer rules. Keep them as reference when you embark upon complex assertions. Annotation in the figure explains the situation(s).

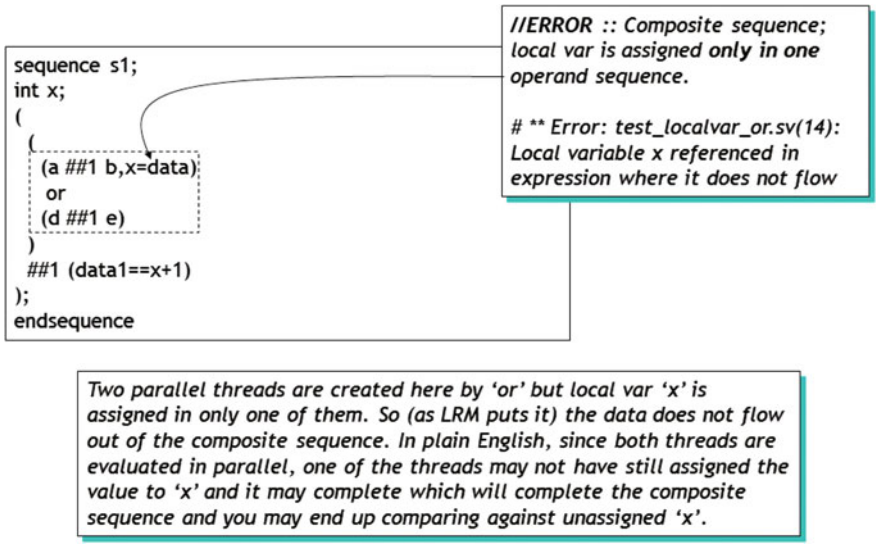


Fig. 9.5 Local variable composite sequence with an 'OR'

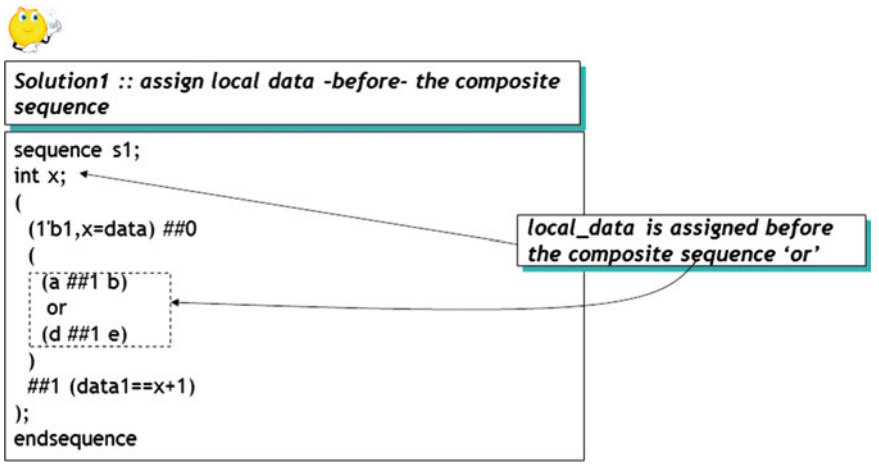


Fig. 9.6 Local variables—for an 'OR' assign local data—before- the composite sequence

Figure 9.6 describes the semantics governing local variables when they are used in the OR of two sequences. The local variable must be assigned in both the sequences of an OR. However, what if you cannot really do that? There are a couple of solutions presented in Fig. 9.7.

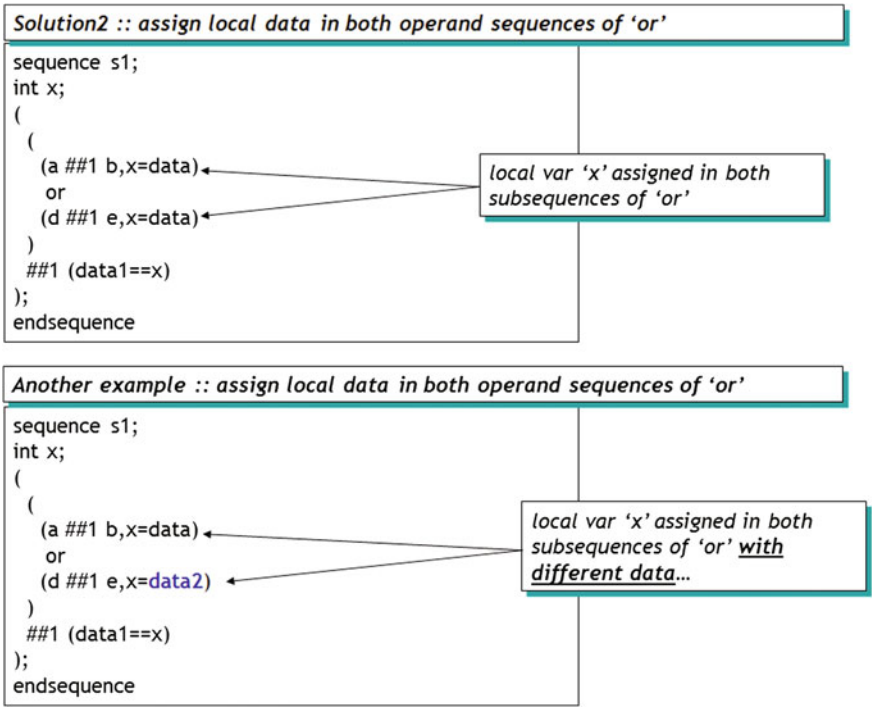


Fig. 9.7 Local variables—assign local data in both operand sequences of 'OR'

Figure 9.9 describes semantics that govern an 'and' of two sequences. In contrast to an 'or' of two sequences, a local variable must *not* be attached to both sequences involved in an 'and'. The first solution is identical to that for an 'or'. Assign the local variable outside of the 'and' of the two sequences as shown in the figure. Alternatively, simply assign to the local variable in only 1 of two sequences, which is an obvious solution. Figure 9.9 shows solution #2 in addition to the solution #1 in Fig. 9.8.

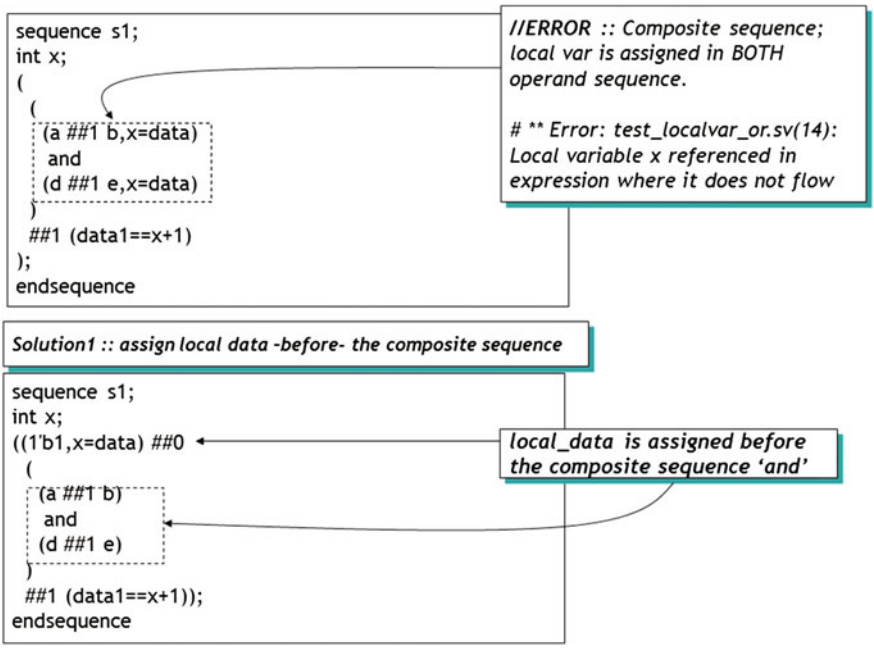


Fig. 9.8 Local variables—'and' of composite sequences

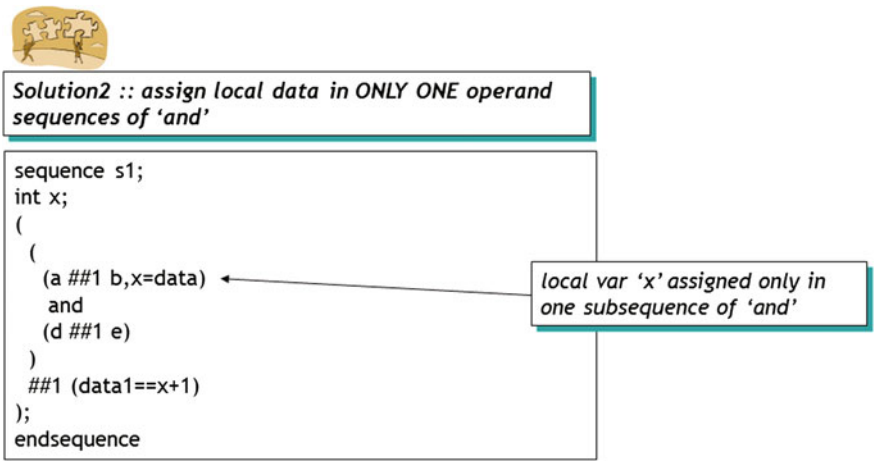


Fig. 9.9 Local variables—finer nuances III

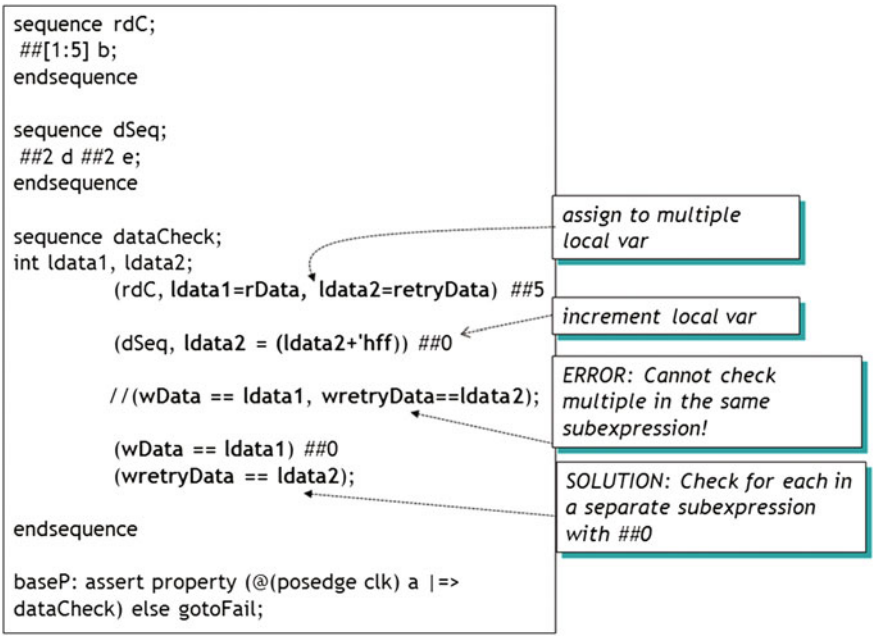


Fig. 9.10 Local variables—further nuances IV

Figure 9.10 describes further rules governing local variables. First, you can assign to multiple local variables, attached to a single expression. Second, you can also manipulate the assigned local data in the same sequence (as is the case for ldata2). But as before, there are differences in assigning to (storing to) local variables and comparing their stored value. *You cannot compare multiple local*

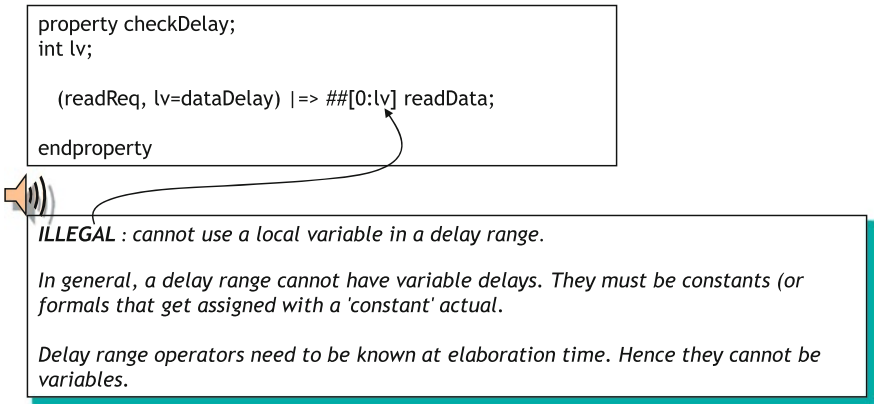


Fig. 9.11 Local variable cannot be used in delay range

variable values in a single expression in a sequence as is the case in the line "//(wData == ldata1, wretryData==!ldata2)". This is illegal. Of course, there is always a solution as shown in the figure. Simply separate comparison of multiple values in two subsequences with no delay between the two. The 'Solution' annotation in the figure makes this clear.

Figure 9.11 shows that you cannot use a local variable in the range operator. But, it's not the local variables fault. It's the fact that we cannot have variable delay in either #m or #[m:n] delay operators. From software point of view, the delay range operators need to be known at elaboration time. Hence they cannot be 'variables'. From hardware point of view, this is a bummer!

Figure 9.12 shows that you cannot use a 'formal' to size a local variable. Again, 'size' of a vector (bus) declaration can only be a constant. Again, there is a software reason and a hardware reason. I will leave it up to the reader to guess what I think!

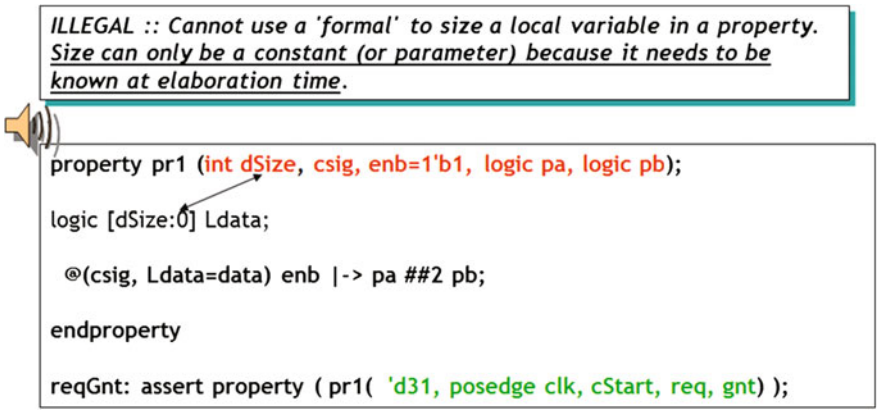


Fig. 9.12 Local variables—cannot use a 'formal' to size a local variable

9.1 Application: Local Variables

Once a 'read' has been issued, another 'read' for the same readID cannot be re-issued until a readAck with the same ID has returned.

```
property checkRead;
  int localID;
  ($rose(read),localID = readID) |=>
                    not (($rose(read) && readID==localID) [*1:$]) ##0
                    ($rose(readAck) && readAckID == localID);
endproperty

baseP: assert property (checkRead) else
                    $display($stime,,,"\tproperty FAIL");
```

Fig. 9.13 Local variables—application

The application in Fig. 9.13 is broken down as follows.

($rose(read),localID=readID

On $rose(read), the readID is stored in the localID.

not (($rose(read) && readID==localID) [*1:$])

Then we check to see if another read ($rose(read)) occurs and it's readID is the same as the one we stored for the previous Read in localID. We continue to check this consecutively until

*##0 ($rose(readAck) && readAckID == localID)*occurs.

If the consecutive check does result in a match, that would mean that we did get another $rose(read) with the same readID with which the previous read was issued. That's a violation of the specs. This is why we take a 'not' of this expression to see that it turns false on a match and the property would end.

If the consecutive check does not result in a match until *##0 ($rose(readAck) && readAckID == localID)* arrives then we indeed got a readAck with the same readAckID with which the original read was issued. The property will then pass.

In short we have proven that once a 'read' has been issued that another 'read' from the same readID cannot be re-issued until a 'readAck' with the same ID has returned.

Chapter 10
Recursive Property

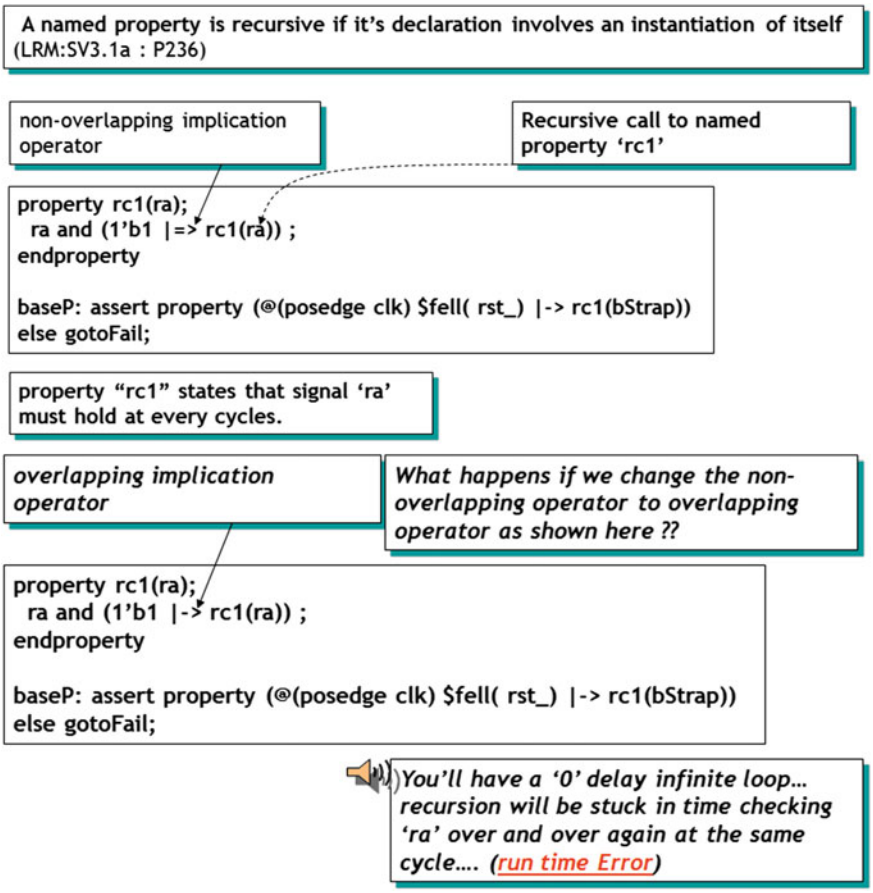


Fig. 10.1 Recursive property—basics

A. B. Mehta, *SystemVerilog Assertions and Functional Coverage*,
DOI: 10.1007/978-1-4614-7324-4_10,

Recursive property simply states that a condition holds. The property calls itself with a correct non-overlapping implication operator and correct antecedent and consequent relation. As shown in Fig. 10.1 (top "property rc1"), if 'ra' is true *and* at next clock rc1(ra) is true that 'rc1' should recur on itself. Note that the antecedent in 'rc1' is 1'b1, meaning the antecedent is always true. This allows for an easy and correct 'and' of an expression with an antecedent/consequent implication. Note also that you must use a non-overlapping operator in a recursive property.

The topmost example in Fig. 10.1 (**baseP: assert property (@ (posedge clk) $fell(rst_) |-> rc1(bStrap)) else gotoFail;**) specifies that when $fell(rst_) is true, the consequent rc1(bStrap) is invoked. 'rc1' property takes 'bStrap' as the input and does an 'and' of the input with (1'b1 |=> rc1(ra)). This means that the implication 1'b1 is always true and that rc1(ra) will be called every posedge of clk to recurs on itself. The property will continue to go into loop on itself until bStrap is sampled 0. In that case the 'and' will fail and so would the property. In other words, we have checked to see that after $fell(rst_), the 'bStrap' (bootstrap signal) does not get de-asserted (i.e. go Low).

Note: If you use an overlapping operator, the property will recurs on itself in zero time, essentially trapping the simulator in a zero delay loop causing simulation to hang.

But, what good does the property in Fig. 10.1 really do. It will check for a signal to hold forever. How do you apply such a model to real world? What you really need to check is that a condition holds until another condition remains true. If that happens, the property passes, else it fails. Now that is more practical. Let us understand this with the following example.

10.1 Application: Recursive Property

As shown in Fig. 10.2, with an 'or' condition, the recursive property becomes useful. The specification says that we need to make sure that 'intr' is held true until 'iack' is asserted. Let's see how that works. property rc1 says that either iack is true or intr is true that the property calls rc1 recursively. Now, if an interrupt arrives—before- and iack, the **(intr and ('true |=> rc1(intr,iack)))** will fail because this is an AND with intr. On the other hand, if iack arrives first, the "iack or…" condition will pass because this is an OR. In other words, we are recursive on 'intr' to see that it holds true until iack arrives.

At time 55 in the simulation log, iack=1 and intr=0. Since intr was equal to '1' the previous clock, it held itself until iack arrived. Hence, the property passes. On the other hand, at time 105, intr goes '0' *before*' iack goes 1. In other words, intr did not hold itself until iack arrived and the property fails. Figure 10.3 shows another interesting application.

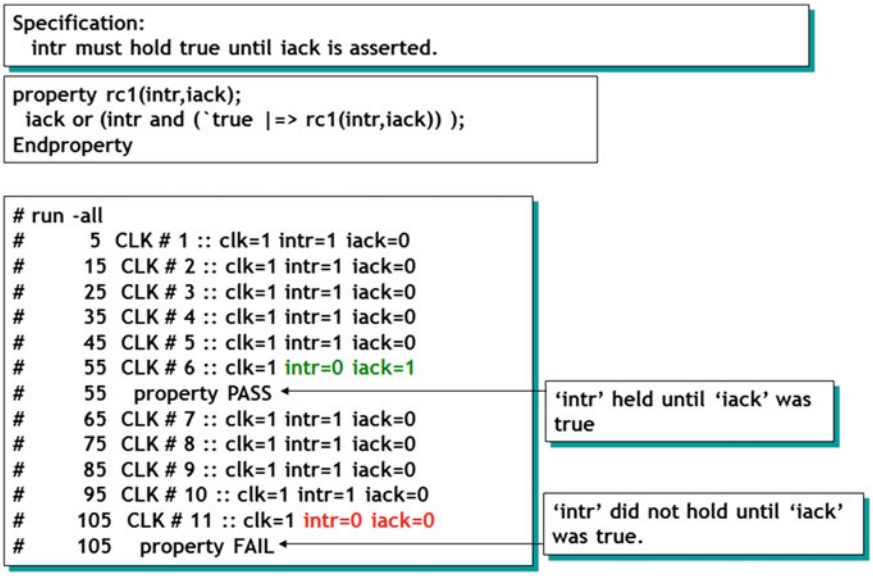


Fig. 10.2 Recursive property—Application

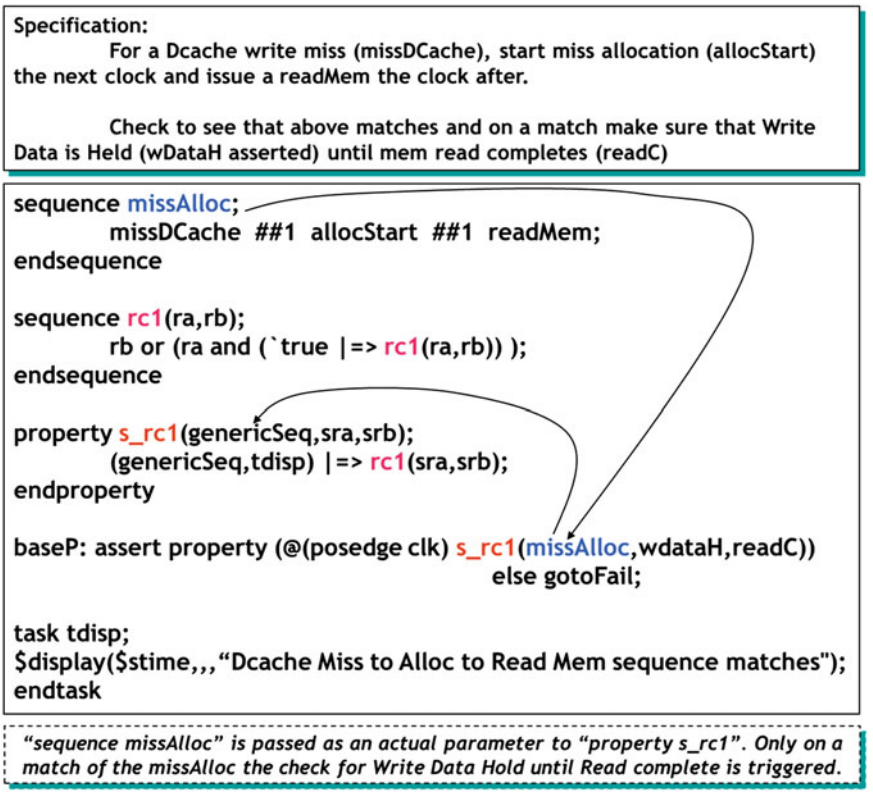


Fig. 10.3 Recursive property—Application

The specification of this property reads as “on detection of missAlloc, see that wdataH is held until readC is true”. In Fig. 10.3, property ‘s_rc1’ checks to see that ‘misAlloc’ is true, upon which it triggers ‘rc1’. Property rc1 in turn holds true (i.e. recursive) until readC is true. If ‘wdataH’ goes low before readC goes high, the property (and hence the entire assertion) will fail (because wdataH is the LHS of an ‘and’ condition in sequence rc1. If readC arrives before wdataH, the ‘or’ condition in the sequence rc1 passes and hence the assertion would pass.

This way we have made sure that wdataH is held until readC completes. If this is not quite apparent at first, please refer to Fig. 10.2 to understand how ‘property rc1’ works.

Note that we are passing the entire sequence ‘missAlloc’ as an actual to the formal ‘genericSeq’ of property s_rc1. This is a very useful way to use a sequence as an actual to sequence formal.

Further nuances are described in Fig. 10.4 with annotations.

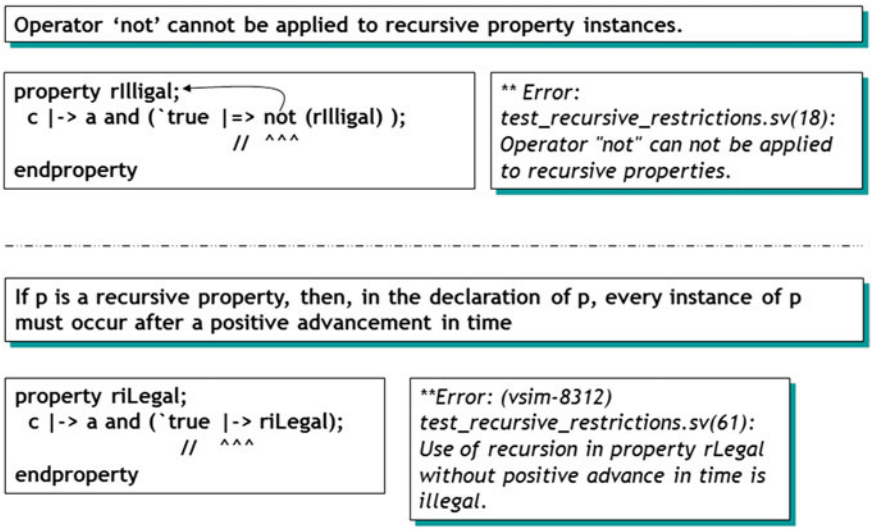


Fig. 10.4 Recursive property—further nuances I

Figure 10.5 shows that ‘disable iff’ is not allowed in a recursive property. Well, there is a simple solution to that problem, which is shown in the bottom of the figure. Separate the requirement of ‘disable iff’ and the recursive nature of the property in two properties. The recursive property does not contain ‘disable iff’ and the ‘property rillegal’ disables rLegal with the ‘disable iff’ condition.

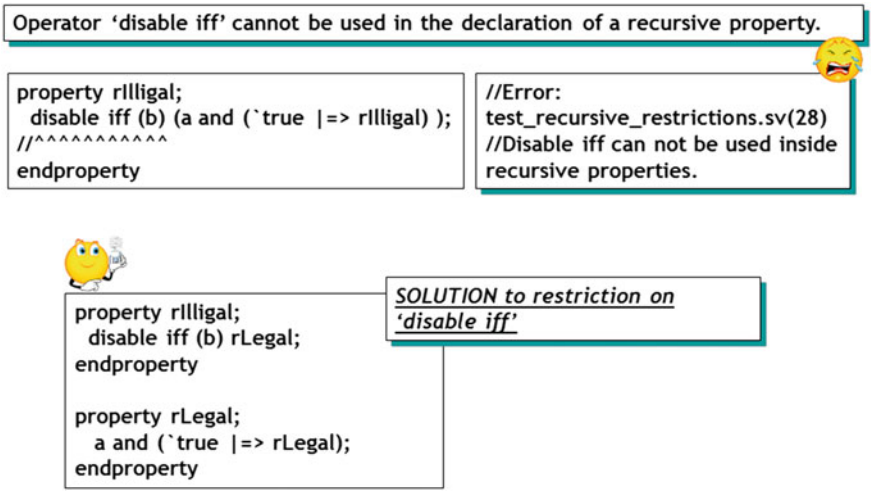


Fig. 10.5 Recursive property—further nuances II

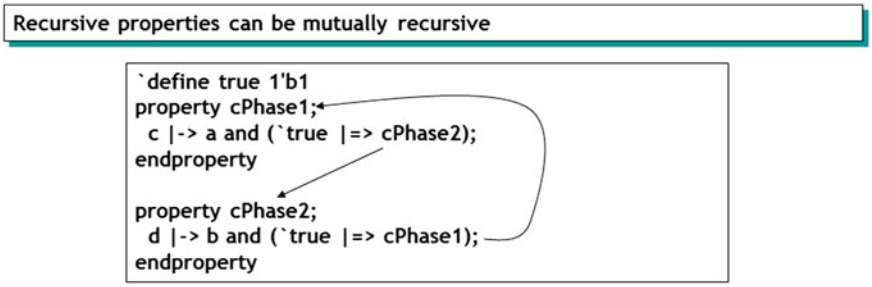


Fig. 10.6 Recursive property—mutually recursive

Figure 10.6 shows that two recursive properties can indeed be mutually recursive. 'cPhase2' calls 'cPhase1' and 'cPhase1' in turn calls 'cPhase2'. Why would this not end up in a zero delay loop? First of all, there is the 1 clock wait because of the non-overlapping operator in both properties. Second, each property has an antecedent and the property will execute only if the antecedent is true. So, if 'cPhase2' calls 'cPhase1', then 'cPhase1' will first wait for 'c' to be true and then trigger the recursive part of the property. The same happens when 'cPhase1' calls 'cPhase2'.

Chapter 11
Detecting and Using Endpoint of a Sequence

11.1 .ended

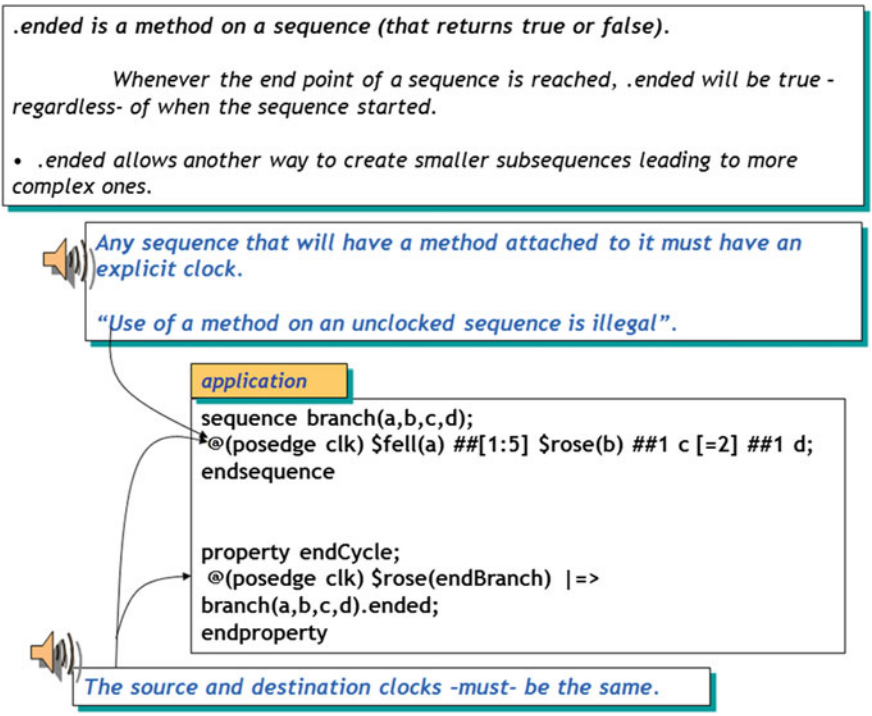


Fig. 11.1 .ended—end point of a sequence

Before we learn how .ended works, here's what has changed in the 1800-2009 standard.

A. B. Mehta, *SystemVerilog Assertions and Functional Coverage*,
DOI: 10.1007/978-1-4614-7324-4_11,

The 2009 standard gets rid of .ended and in place supports .triggered. In other words, .triggered has the same exact meaning as .ended, only that .triggered can be used both where .ended gets used as well as where .triggered was allowed in previous versions. In other words, .triggered can be used in a sequence as well as in procedural block and also in level sensitive 'wait' statement.

Following from the 1800-2009 LRM:

IEEE Std 1800-2005 17.7.3 required using the .ended sequence method in sequence expressions and the .triggered sequence method in other contexts. Since these two constructs have the same meaning but mutually exclusive usage contexts, in this version of the standard, the .triggered method is allowed to be used in sequence expressions, and the usage of .ended is deprecated and does not appear in this version of the standard.

I will still go ahead and explain how .ended works, in case you have not switched to 1800-2009.

Ok, continuing with .ended…

If you are mainly interested in the *end* of a sequence regardless of when it started, .ended is your friend. The main advantage of methods that detect the endpoint of a sequence is that you do not need to know the start of the sequence. All you care for is, when a sequence ends.

Figure 11.1 shows that behavior. Sequence 'branch' is a complete sequence for a branch to complete. It could have started any time. The property endCycle wants to make sure that the 'branch' sequence has indeed ended when endBranch flag goes high. In other words, whenever $rose(endBranch) is detected to be true that the next clock, branch must end. This is indeed very powerful and useful feature. This makes the assertion intuitive as well.

But what if you simply write the assertion as "at the end of 'branch' see that endBranch goes high" as in "branch (a, b, c, d) |=> $rose(endBranch)". What's wrong with that? Well, what if $rose(endBranch) goes high when the 'branch' is still executing? That $rose(endBranch) would go unnoticed until the end of the sequence 'branch'. The .ended operator would catch this. If endBranch goes high when sequence 'branch' is still executing, the property will fail. That's because the property endCycle expects 'branch' to have ended when endBranch goes high. Since endBranch could have risen prematurely, the property will see that at $rose(endBranch) the 'branch' sequence has not ended and the property would fail. The forward looking property would not catch this. This is a very important point. Please make a note of it.

Also, note that the clock in both the source and destination sequence must be the same. But what if you want the source and destination clocks to be different? That is what '.matched' does, soon to be discussed.

Figure 11.2 explains further nuances.

```
sequence aRb(aFell,bRose);
 @(posedge clk) $fell(aFell) ##1 $rose(bRose);
endsequence

property endCycle;
          @(posedge clk) $rose(c) |-> aRb(a,b).ended;
endproperty
baseP: assert property (endCycle) else gotoFail;
```

overlapping implication

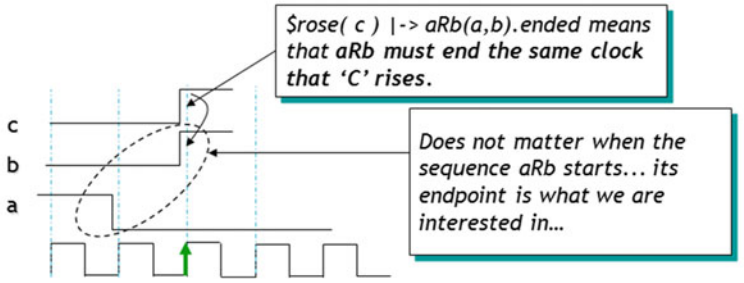


Fig. 11.2 .ended with overlapping operator

In the example, $rose(c) implies that the sequence aRb must have ended. Key point to note here is that the implication operator is overlapping. This means that when $rose(c) occurs that at the same clock, sequence aRb should end. As shown in Fig. 11.2, when $rose(c) is true that at the same clock $rose(b) must occur and the previous clock $fell(a).

Figure 11.3 describes the same example but with the non-overlapping operator.

```
sequence aRb(aFell,bRose);
 @(posedge clk) $fell(aFell) ##1 $rose(bRose);
endsequence

property endCycle;
          @(posedge clk) $rose(c) |=> aRb(a,b).ended;
endproperty
baseP: assert property (endCycle) else gotoFail;
```

non-overlapping implication

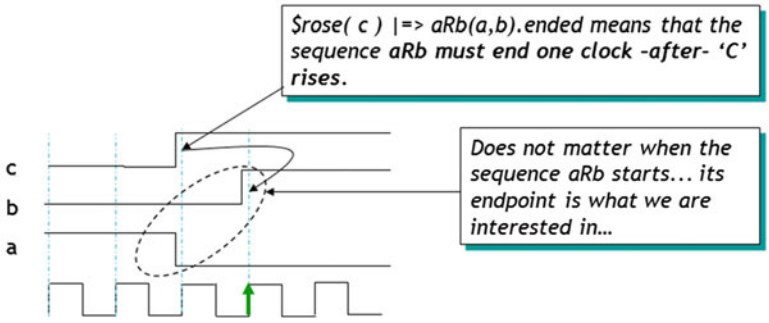


Fig. 11.3 .ended with non-overlapping operator

You have to understand this very carefully, as simple as it looks. Non-overlapping states that when $rose(c) is true that *at the next clock* the sequence aRb must end. Hence, as shown is the figure, the property looks for aRb to end one clock *after* $rose(c). This is intuitive but easy to miss.

11.2 .matched

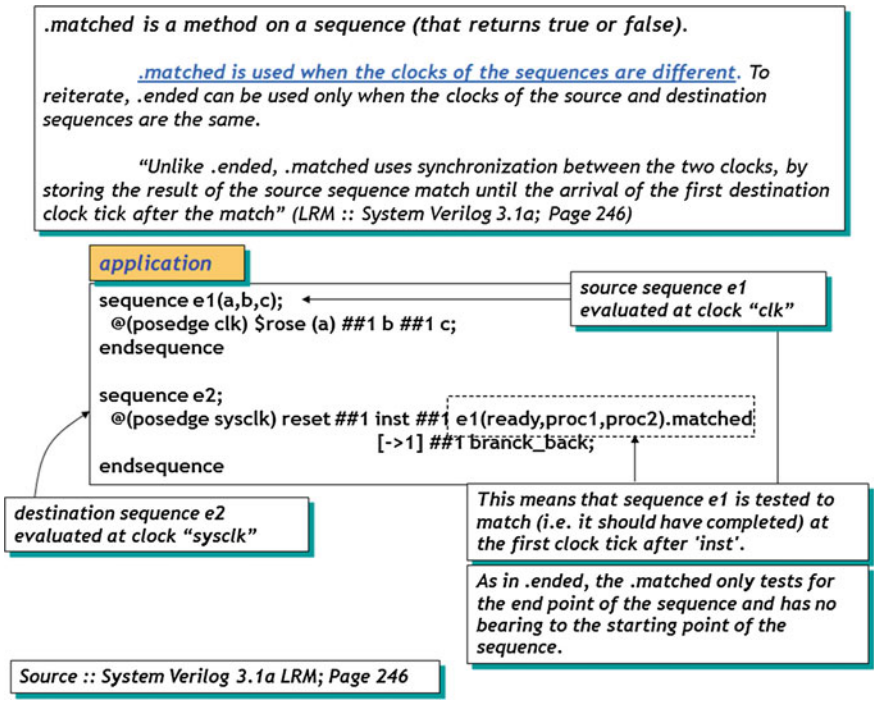


Fig. 11.4 .matched—basics

The main difference between .ended and .matched is that .ended requires both the source and destination sequences to have the same clock. .matched allows you to have different clocks in the source and destination sequences.

Since the clocks can be different, understanding of .matched gets a bit complicated. But it follows the same rules as that for multiply clocked properties. As shown in Fig. 11.4, sequence 'e1' uses 'clk' as its clock while sequence 'e2' uses 'sysclk' as it's clock. Sequence 'e2' says that after 'reset'; 1 clock later; 'inst' must be true and 1 clock later sequence 'e1' must match (i.e. end) at least once and 1 clock later branch_back must be true. This is very interesting way of 'inserting' a .matched (or .ended for that matter) within a sequence. Sequence 'e1' is running on its own. What we really care for is that it matches (ends) when we expect it to.

Let us look at some examples that will make the concept clear.

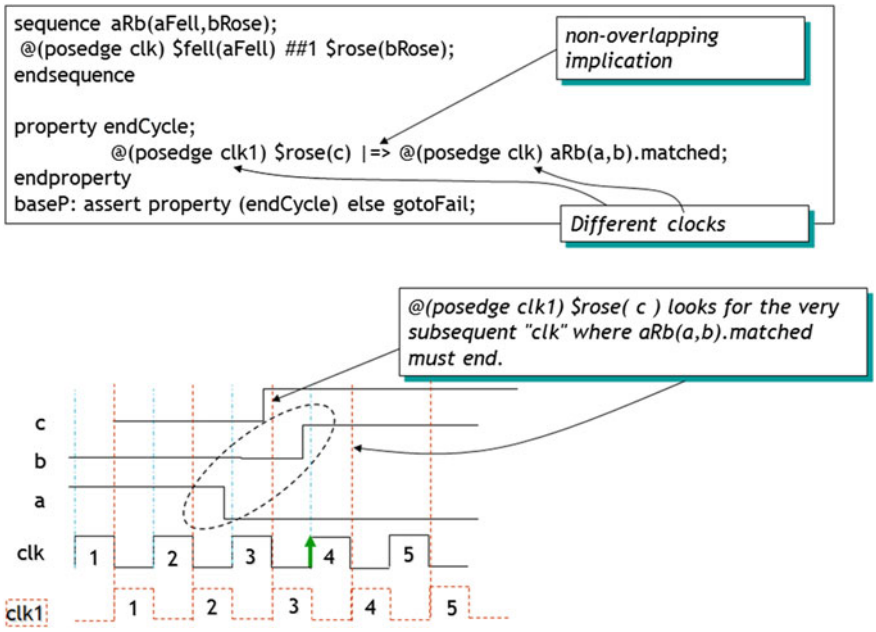


Fig. 11.5 .matched with non-overlapping operator

Figure 11.5 shows that on the rising edge of 'c' we want to see that aRb sequence matches. Let us look at the timing diagram. When, $rose(c) is true at posedge of clk1 (clk1=3), it looks for the end of the sequence 'aRb'. Sequence 'aRb' started during clk=3 and it ends at clk=4. Note that the end of 'aRb' (i.e. match of $rose(bRose)) is exactly at the very *next* 'clk' edge after clk1 edge. That's what the property asked for "@ posedge clk1) $rose(c) |=> @ (posedge clk) aRb(a,b).matched;"

The key point to note here (as in multiply clocked properties) is the clock crossing boundary. From clk1 to clk with 1 clock delay in-between (as implied by |=> non-overlapping implication) does not mean 1 full clock. It simply means the *very next edge* of 'posedge clk' after 'posedge clk1'. Please refer to multiply clocked properties (Sect. 8.1) if this concept is not clear.

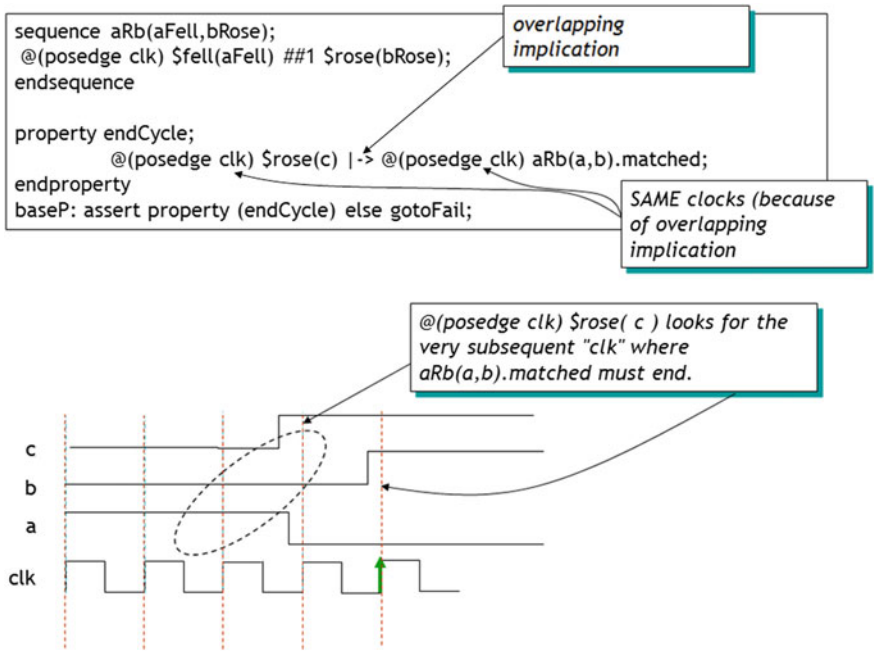


Fig. 11.6 .matched—overlapped operator

Figure 11.6 uses overlapped implication and identical (in-phase) clocks (the clocks have to be the same because we are using overlapping implication). Hence when $rose(c) is true, it looks for the very *next* (posedge clk) overlapping with its (posedge clk). But the very next (posedge clk) is (obviously) 1 clock later. So, 1 clock after $rose(c), the sequence sees that aRb has matched (i.e., .ended).

11.2.1 Application: .matched

```
sequence RdS;
  @(posedge Busclk) $fell (as_) ##1 rd ##[1:5] oe_;
endsequence

property checkP;
  @(negedge sysclk) RdS.matched  |=> rdDataLatch ##0 ($isunknown
(data) == 0);
endproperty
```

The matched value of sequence RdS is sampled at the negedge of sysclk and if it is true (i.e. the sequence has completed) it implies that rdDataLatch is asserted the next negedge sysclk and that the data is not unknown at that clock

Fig. 11.7 .matched—application

In Fig. 11.7, sequence 'RdS' uses Busclk while the property checkP uses sysclk. "@ (negedge sysclk) RdS.matched" means that at the negedge of sysclk, the sequence RdS (which is running off of Busclk) must end. 'RdS' could have completed slightly (i.e., when the very preceding posedge of Busclk would have arrived) earlier than the negedge sysclk. That is ok because we are transitioning from Busclk to sysclk (as long as the sequence RdS completes at the immediately preceding posedge Busclk).

Chapter 12
'expect'

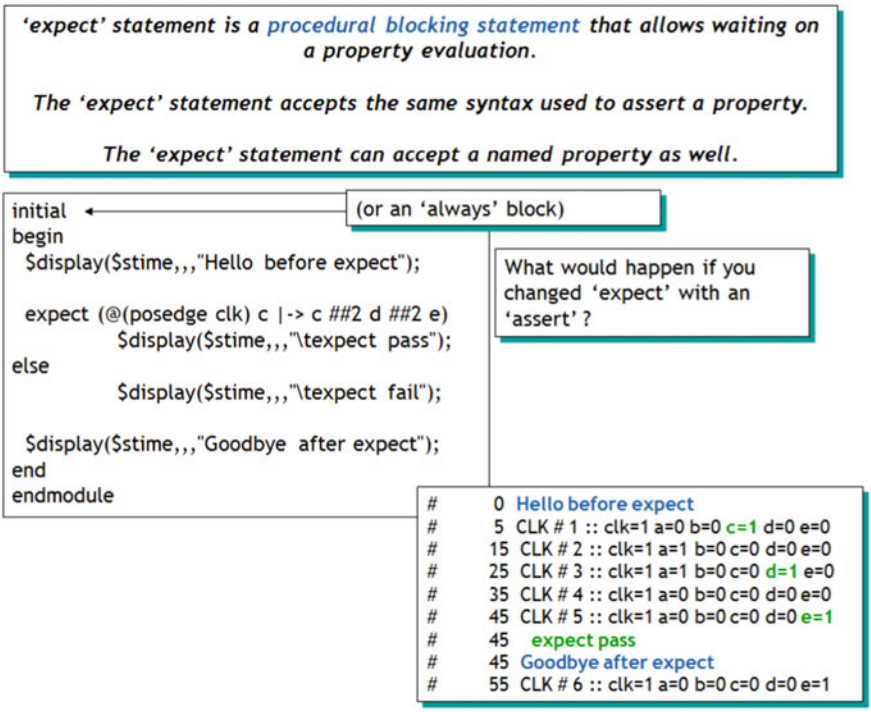


Fig. 12.1 'expect'—basics

'expect' takes on the same syntax (not semantics) as 'assert' in a procedural block. *Note that 'expect' must be used only in a procedural block*. It cannot be used outside of a procedural block as in assert/property/sequence—but recall that 'assert' can be used both in the procedural block as well as outside. So, what's the difference between 'assert' and 'expect'?

A. B. Mehta, *SystemVerilog Assertions and Functional Coverage*,
DOI: 10.1007/978-1-4614-7324-4_12,

'expect' is a blocking statement while 'assert' is a non-blocking statement. Blocking means the procedural block will wait until 'expect' sequence completes (pass or fail). For 'assert' non-blocking means that the procedural block will trigger the 'assert' statement and continue with the next statement in the block. 'assert' condition will continue to execute in parallel to the procedural code. Note that 'assert' behavior is the same whether it's outside or inside a procedural block. It always executes in parallel on its own thread with the rest of the logic.

Please refer to the simulation log in Fig. 12.1. You notice that the procedural code waits for 'expect' to complete (i.e. blocks execution of procedural code) and only on completion of 'expect' that it executes the subsequent $display. Figure 12.2 highlights further nuances of 'expect' semantics. Annotations in the figure are self-explanatory. *Key point is that 'expect' does not inherit a clock from its preceding procedural clock*. It needs an explicit clock in the sequence (or property) it 'expects' or with its own declaration.

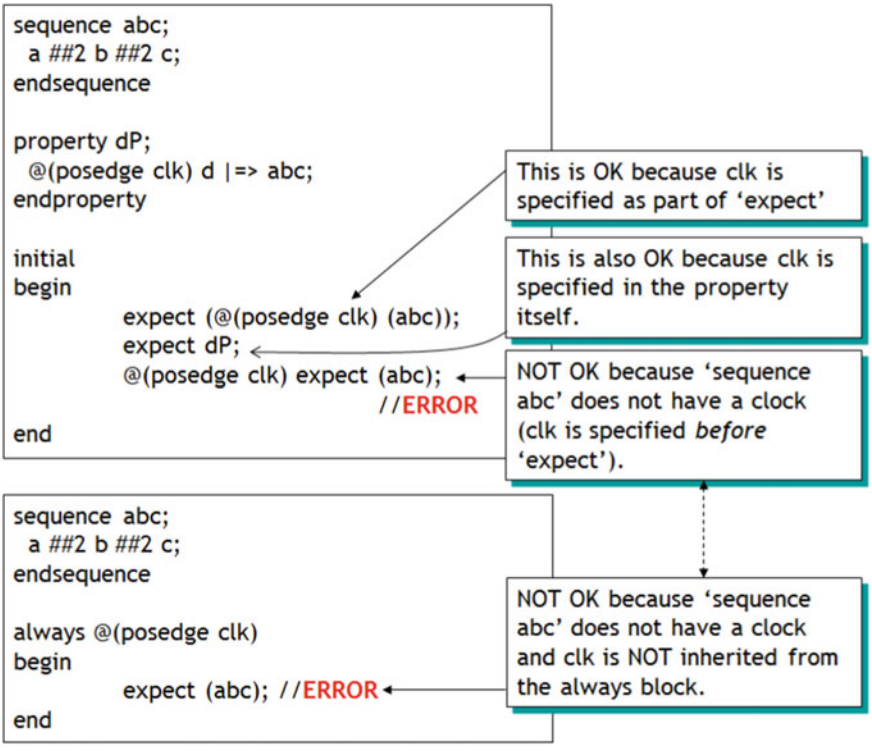


Fig. 12.2 'expect'—error conditions

Chapter 13
'assume' and Formal (Static Functional) Verification

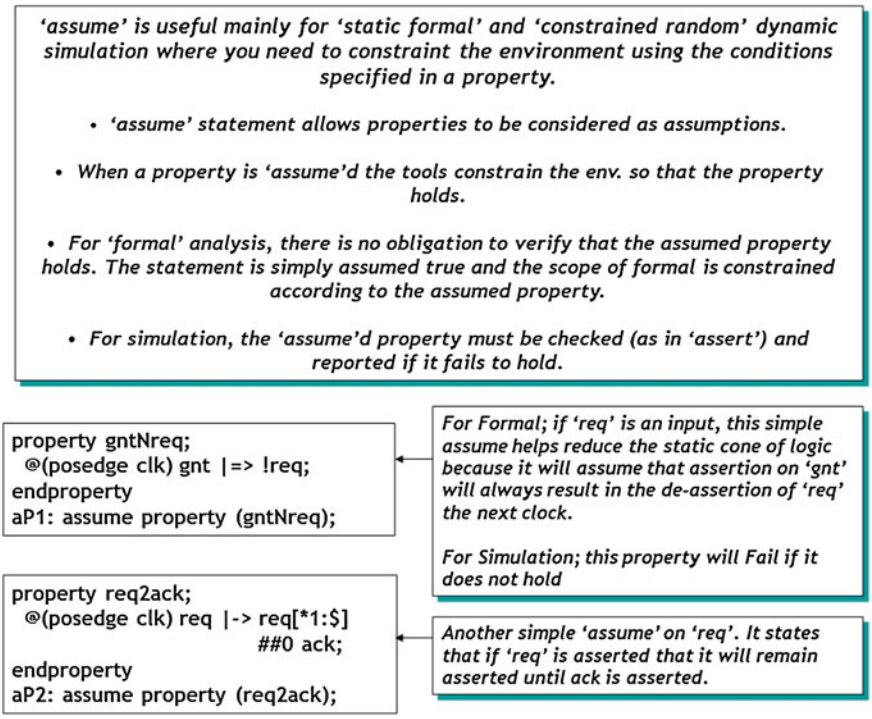


Fig. 13.1 'Assume' and formal verification

This is an interesting operator. 'assume' specifies the property as an assumption for the environment. What's an environment? The most useful 'environment' for 'assume' is that of static formal verification. Static formal is a method whereby the formal algorithm exercises all possible combinational and sequential possibilities of inputs to exercise all possible 'logic cones' of a given logic block and checks to

A. B. Mehta, *SystemVerilog Assertions and Functional Coverage*,
DOI: 10.1007/978-1-4614-7324-4_13,

see that the assertion holds. During such verification if you do not specify any constraints (i.e. for a 5 input (a, b, c, d, e) block, if you don't specify any constraints such as 'assume' a=0 and b=1) then the static formal will try to explore all possible combinations of the 5 input both in combinatorial and temporal (if required) domain. Without any constraints provided via 'assume', the static formal tool may experience something called 'state space explosion'. As the description suggests, the tool may give up if too many inputs are unconstrained. This is where the 'assume' statement comes into picture.

So, how does it behave in simulation? The examples in Fig. 13.1 simply shows that 'assume' without any other property reliant on assumed property will act like 'assert'. If the property associated with the assume statement is found to be false, the simulation fails.

Chapter 14
Other Important Topics

14.1 Asynchronous FIFO Assertions

Asynchronous FIFO (compared to synchronous FIFO) is a difficult proposition when it comes to writing assertions. The Read and the Write clocks are asynchronous which means the most important property to check for is data transfer from Write to Read clock. Other assertions are to check for fifo_full, fifo_empty, etc. conditions.

First we present a comprehensive design of the asynchronous fifo. A bit complicated but you don't need to go into its detail. Next we see a test-bench within which I have designed the assertions. Yes, you can have assertions in the design (RTL) (but not recommended), test-bench (as in this example), in a systemverilog Interface, in a systemverilog Program and in a file on its own (this is where the 'bind' comes into picture (this is highly recommended)).

This FIFO design and test-bench are available on Springer server.

14.1.1 FIFO Design

```
module asynchronous_fifo (
    // Outputs
    fifo_out, full, empty,
    // Inputs
    wclk, wclk_reset_n, write_en,
    rclk, rclk_reset_n, read_en,
    fifo_in
);
```

A. B. Mehta, *SystemVerilog Assertions and Functional Coverage*,
DOI: 10.1007/978-1-4614-7324-4_14,

```
parameter    D_WIDTH = 20;
parameter    D_DEPTH = 4;
parameter    A_WIDTH = 2;

input              wclk_reset_n;
input              rclk_reset_n;
input              wclk;
input              rclk;
input              write_en;
input              read_en;
input [D_WIDTH-1:0]    fifo_in;

output [D_WIDTH-1:0]    fifo_out;
output             full;
output             empty;

reg [D_WIDTH-1:0]      reg_mem[0:D_DEPTH-1];
reg [A_WIDTH:0]        wr_ptr;
reg [A_WIDTH:0]        wr_ptr_gray;
reg [A_WIDTH:0]        wr_ptr_gray_rclk_q;
reg [A_WIDTH:0]        wr_ptr_gray_rclk_q2;
reg [A_WIDTH:0]        rd_ptr;
reg [A_WIDTH:0]        rd_ptr_gray;
reg [A_WIDTH:0]        rd_ptr_gray_wclk_q;
reg [A_WIDTH:0]        rd_ptr_gray_wclk_q2;

reg                    full;
reg                    empty;

wire [A_WIDTH:0]       nxt_wr_ptr;
wire [A_WIDTH:0]       nxt_rd_ptr;
wire [A_WIDTH:0]       nxt_wr_ptr_gray;
wire [A_WIDTH:0]       nxt_rd_ptr_gray;
wire [A_WIDTH-1:0]     wr_addr;
wire [A_WIDTH-1:0]     rd_addr;
wire                   full_d;
wire                   empty_d;
```

```
assign wr_addr = wr_ptr[A_WIDTH-1:0];
assign rd_addr = rd_ptr[A_WIDTH-1:0];

always @ (posedge wclk)
  if (write_en) reg_mem[wr_addr] <= #`FF_DLY fifo_in;

assign fifo_out = reg_mem[rd_addr];

always @ (posedge wclk or negedge wclk_reset_n)
  if (!wclk_reset_n) begin
    wr_ptr <= #`FF_DLY {A_WIDTH+1{1'b0}};
    wr_ptr_gray <= #`FF_DLY {A_WIDTH+1{1'b0}};
  end else begin
    wr_ptr <= #`FF_DLY nxt_wr_ptr;
    wr_ptr_gray <= #`FF_DLY nxt_wr_ptr_gray;
  end

assign nxt_wr_ptr = (write_en) ? wr_ptr+1 : wr_ptr;
assign nxt_wr_ptr_gray = ((nxt_wr_ptr>>1) ^ nxt_wr_ptr);

always @ (posedge rclk or negedge rclk_reset_n)
  if (!rclk_reset_n) begin
    rd_ptr <= #`FF_DLY {A_WIDTH+1{1'b0}};
    rd_ptr_gray <= #`FF_DLY {A_WIDTH+1{1'b0}};
  end else begin
    rd_ptr <= #`FF_DLY nxt_rd_ptr;
    rd_ptr_gray <= #`FF_DLY nxt_rd_ptr_gray;
  end

assign nxt_rd_ptr = (read_en) ? rd_ptr+1 : rd_ptr;
assign nxt_rd_ptr_gray = (nxt_rd_ptr>>1) ^ nxt_rd_ptr;

// check full
always @ (posedge wclk or negedge wclk_reset_n)
  if (!wclk_reset_n)
     {rd_ptr_gray_wclk_q2, rd_ptr_gray_wclk_q} <= #`FF_DLY
 {{A_WIDTH+1{1'b0}}, {A_WIDTH+1{1'b0}}};
  else
```

```
      {rd_ptr_gray_wclk_q2, rd_ptr_gray_wclk_q} <= #`FF_DLY
  {rd_ptr_gray_wclk_q, rd_ptr_gray};

  assign full_d = (nxt_wr_ptr_gray == {~rd_ptr_gray_wclk_q2[A_WIDTH:
A_WIDTH-1], rd_ptr_gray_wclk_q2[A_WIDTH-2:0]});

  always @ (posedge wclk or negedge wclk_reset_n)
    if (!wclk_reset_n)
      full <= #`FF_DLY 1'b0;
    else
      full <= #`FF_DLY full_d;

  // check empty
  always @ (posedge rclk or negedge rclk_reset_n)
    if (!rclk_reset_n)
      {wr_ptr_gray_rclk_q2, wr_ptr_gray_rclk_q} <= #`FF_DLY
  {{A_WIDTH+1{1'b0}}, {A_WIDTH+1{1'b0}}};
    else
      {wr_ptr_gray_rclk_q2, wr_ptr_gray_rclk_q} <= #`FF_DLY
  {wr_ptr_gray_rclk_q, wr_ptr_gray};

  assign empty_d = (nxt_rd_ptr_gray == wr_ptr_gray_rclk_q2);

  always @ (posedge rclk or negedge rclk_reset_n)
    if (!rclk_reset_n)
      empty <= #`FF_DLY 1'b1;
    else
      empty <= #`FF_DLY empty_d;

endmodule
```

14.1.2 FIFO Test-Bench and Assertions

```
module test_asynchronous_fifo
(
      fifo_out, full, empty,
      wclk, wclk_reset_n, write_en,
```

```
    rclk, rclk_reset_n, read_en,
    fifo_in
);

  parameter   D_WIDTH = 20;
  parameter   D_DEPTH = 4;
  parameter   A_WIDTH = 2;

  output            wclk_reset_n;
  output            rclk_reset_n;
  output            wclk;
  output            rclk;
  output            write_en;
  output            read_en;

  output [D_WIDTH-1:0]  fifo_in;

  logic             wclk_reset_n;
  logic             rclk_reset_n;
  logic             wclk;
  logic             rclk;
  logic             write_en;
  logic             read_en;
  logic [D_WIDTH-1:0]  fifo_in;

  input [D_WIDTH-1:0] fifo_out;
  input             full;
  input             empty;

asynchronous_fifo aff1
(
    fifo_out, full, empty,
     wclk, wclk_reset_n, write_en,
     rclk, rclk_reset_n, read_en,
     fifo_in
);

/*
```

Following property checks to see that if the FIFO is empty that the wr_ptr does not change.

This assertion can be written other ways too (using for example 'empty' condition). Please try them out and see if the results match with this assertion.

```
*/
property check_full;
  @ (posedge wclk) disable iff (!wclk_rstn)
      (full) |=> @ (posedge wclk) aff1.wr_ptr == $past(aff1.wr_ptr);
endproperty
cfull : assert property (check_full) else $display($stime,,,"%m Check wr_ptr full
  FAIL");
cfullc : cover property (check_full) $display($stime,,,"%m Check wr_ptr full
  PASS");

/*
```

Following property checks to see that if the FIFO is empty that the rd_ptr does not change. 'empty' means that the rd_ptr remains the same as its value at the last clk—thus guaranteeing that the rd_ptr have not changed. BUT note that we are using !$isunknown and passing it $past as an expression. Why? If FIFO is empty, the rd_ptr in the past could be 'X'. So we make sure that rd_ptr is the same as the past value and that it is not unknown.

This assertion can be written other ways too (using for example 'full' condition or without the use of $past). Please try them out and see if the results match with this assertion.

```
*/
property check_empty;
  @ (posedge rclk) disable iff (!rclk_rstn)
      (empty) |=> @ (posedge rclk)
          if (!$isunknown($past(aff1.rd_ptr)))
           (aff1.rd_ptr == $past(aff1.rd_ptr));
endproperty
cempty : assert property (check_empty) else $display($stime,,,"%m Check rd_ptr
  empty FAIL");
cemptyc : cover property (check_empty) $display($stime,,,"%m Check rd_ptr
  empty PASS");
```

```
/*-----------------------------------------
  ASYNCHRONOUS DATA TRANSFER CHECK
-----------------------------------------*/
/*
```

This is a very important assertion for an asynchronous FIFO. Check that the data that is written at a wr_ptr is the same data that is read when rd_ptr reaches that wr_ptr. Simple! Let us look at the assertion step by step

```
*/
/*
```

In the assertion, data_check property checks to see that FIFO is not full. If so, saves wr_ptr into the local variable 'ptr' and the data from fifo into local variable 'data' and display that so that we can easily see how the assertion is progressing during simulation.

If the antecedent is true, the consequent says that the first match of rd_ptr being the same as wr_ptr (note wr_ptr was stored in local variable ptr) that the read data is the same as the write data (note write data were stored in local variable data in the antecedent).

Sequence rd_detect(ptr) is used as an expression to first_match. It says that wait from now until forever until you detect a read and it's rd_ptr is equal to the wr_ptr (which is stored in the local variable 'ptr' in the antecedent).

Please note that these are multi-clocked properties since we have a wr_clk and a rd_clk.

So, in this property, we see

- multi-clock property (wclk and rclk)
- use of local variables for storing/comparing
- first_match
- attaching a subroutine (here a $display) to an expression for effective debugging
- effective use of ##0 to create overlapping condition in a sequence.

Try out different ways to write the assertion. Refer to different operators, sampled value functions etc. and see if you can write an equivalent assertion. There isn't just one way to write an assertion. But there is indeed a right way and a wrong way. You will get that through practice.

```
*/
sequence rd_detect(ptr);
  ##[0:$] (read_en && !empty && (aff1.rd_ptr == ptr));
endsequence
```

```
property data_check(wrptr);
integer ptr, data;
  @ (posedge wclk) disable iff (!wclk_reset_n || !rclk_reset_n)
          (write_en && !full, ptr=wrptr, data=fifo_in,
    $display($stime,"\t Assertion Disp wr_ptr=%h data=%h",aff1.wr_ptr,fifo_in))

|=>

  @ (negedge rclk) first_match(rd_detect(ptr),
    $display($stime,,," Assertion Disp FIRST_MATCH ptr=%h Compare data=%h
      fifo_out=%h", ptr, data, fifo_out))
          ##0 (fifo_out === data);
endproperty

dcheck : assert property (data_check(aff1.wr_ptr)) else  $display($stime,,,"FAIL:
   DATA CHECK");
dcheckc : cover property (data_check(aff1.wr_ptr)) $display($stime,,,"PASS:
   DATA CHECK");

/*-----------------------------------------
  If FULL -> NOT EMPTY Check
-----------------------------------------*/
/*
```

Following property is quite self-explanatory. But note that this is also a multi-clocked property and since the write and read clocks are different clocks, we must use the non-overlapping operator |=> .

This is a mutex property. What are the different ways you can write this?

```
 */
 property full_empty;
  @ (posedge wclk) disable iff (!wclk_reset_n)
          @ (posedge wclk) (full) |=> @ (posedge rclk) (!empty);
 endproperty

 few :assert property (full_empty) else $display($stime,," FAIL: Full and Empty
    BOTH asserted");
 cfew : cover property (full_empty) $display($stime,," PASS: Full and Empty
    check");
```

```
/*-----------------------------------------
  If EMPTY -> NOT FULL Check
-----------------------------------------*/
/*
```

Following property is quite self-explanatory. But note that this is also a multi-clocked property and since the write and read clocks are different clocks, we must use the non-overlapping operator |=> .

This is a mutex property. What are the different ways you can write this?

```
*/
property empty_full;
 @ (posedge wclk) disable iff (!wclk_reset_n)
        @ (posedge rclk) (empty) |=> @ (posedge wclk) (!full);
endproperty

efw : assert property (full_empty) else $display($stime,,, "FAIL: Full and Empty
   BOTH asserted");

/*-----------------------------------------
  rclk_reset_n Check on rclk
-----------------------------------------*/
/*
```

Following property checks to see that empty pointer is high (i.e. empty) when you reset the FIFO

```
 */
 property reset_n_rclk;
   @ (posedge rclk) !rclk_reset_n |-> empty;
 endproperty

 reset_nrclkA: assert property (reset_n_rclk) else $display($stime,,,"FAIL: FIFO
 not empty during rclk_reset_n");
 reset_nrclkC: cover property (reset_n_rclk) $display($stime,,,"PASS: FIFO
 empty during rclk_reset_n");

 /*-----------------------------------------
   wclk_reset_n Check on wclk
 -----------------------------------------*/
 /*
```

Following property checks to see that the FIFO is not full when you reset the FIFO. FIFO can only go Empty during reset, not Full.

```
*/

property reset_n_wclk;
  @ (posedge wclk)  !wclk_reset_n |-> !full;
endproperty

reset_nwclkA: assert property (reset_n_wclk) else $display($stime,,,"FAIL:
   FIFO FULL during wclk_reset_n");
reset_nwclkC: cover property (reset_n_wclk) $display($stime,,,"PASS: FIFO
   FULL during rclk_wstn");
```

14.1.3 Test the Test-bench

```
/*
```

Following assertions are important to note. We are checking our own test-bench! Yes, that is important. This is a simple test-bench but the idea is that as your test-bench develops complex code that there is a good chance you will make mistakes. So why not use assertions to catch those errors as well.

For example, in the first assertion we are checking that if FIFO is full that we do not keep writing to it, since this particular FIFO does not have a pushback signal.

Similarly the second assertion checks to see that if the FIFO is empty that we do not keep reading it!

```
*/

/*-----------------------------------------
  Checks for the Test-bench
-----------------------------------------*/
property check_full_write_en;
  @ (posedge wclk) disable iff (!wclk_reset_n)
        full |-> !write_en;
endproperty

check_full_write_enA : assert property (check_full_write_en) else
$display($stime,,,"%m FAIL: check_full_write_en");
```

```
check_full_write_enC : cover property (check_full_write_en)
$display($stime,"%m PASS: check_full_write_en");

property check_empty_read_en;
  @ (posedge rclk) disable iff (!rclk_reset_n)
        empty |-> !read_en;
endproperty

check_empty_read_enA: assert property (check_full_write_en) else
$display($stime,,,"FAIL: %m check_full_write_en");
check_empty_read_enC: cover property (check_full_write_en)
$display($stime,,,"PASS: %m check_full_write_en");

integer i, seed1, wclk_width, rclk_width, loopcount, base;

/*
Following is regular Verilog test-bench code which you are very familiar with


*/

initial begin
 loopcount = 50;
 seed1 = 12345;
 wclk = 1'b1; write_en=1'b1;
 rclk = 1'b0; read_en=1;

 fork
 begin wclk_reset_n = 1'b0; #100; wclk_reset_n = 1'b1; write_en=1'b1; end
 begin rclk_reset_n = 1'b0; #100; rclk_reset_n = 1'b1; read_en=1'b0; end

 for (i=0; i<loopcount; i++)
 begin
  //rclk_width = ({$random} % 40) + 5;
  //wclk_width = ({$random} % 40) + 5;

  rclk_width = 40; wclk_width = 40;
  //rclk_width = 10; wclk_width = 40;
  //rclk_width = 40; wclk_width = 10;
```

```
   $display($stime,,,"wclk_width=%0d rclk_width=%0d",wclk_width,rclk_width);
   #1000#i;
  end
  join

  $finish(2);
end

always #rclk_width rclk=!rclk;
always #wclk_width wclk=!wclk;

always @ (wclk,rclk,write_en,read_en,full,empty,aff1.wr_ptr,aff1.
   rd_ptr,fifo_in,fifo_out)
begin
            $strobe($stime,,,"\t\twclk=%b rclk=%b write_en=%b read_en=%b
full=%b empty=%b wr_ptr=%d rd_ptr=%d fifo_in=%h fifo_out=%h",
                        wclk,rclk,write_en,read_en,full,empty,aff1.wr_ptr,aff1.
            rd_ptr,fifo_in,fifo_out);
end

always @ (negedge wclk) begin
  if (rclk_reset_n) begin
   if (!full) begin
      write_en=1'b1;
      fifo_in = $random({seed1});
     end
   else
     write_en=1'b0;
  end
end

always @ (posedge rclk) begin
  #2;
  if (rclk_reset_n) begin
   if (!empty) begin
     read_en=1'b1;
     //$strobe($stime,,,"READ: Pointer=%h data=%h",aff1.rd_ptr,fifo_out);
```

```
    end
   else
    read_en=1'b0;
  end
end

always @ (wclk_reset_n) $strobe($stime,,,"\twclk_reset_n=%b",wclk_reset_n);
always @ (rclk_reset_n) $strobe($stime,,,"\trclk_reset_n=%b",rclk_reset_n);

endmodule
```

14.2 Embedding Concurrent Assertions in Procedural Code

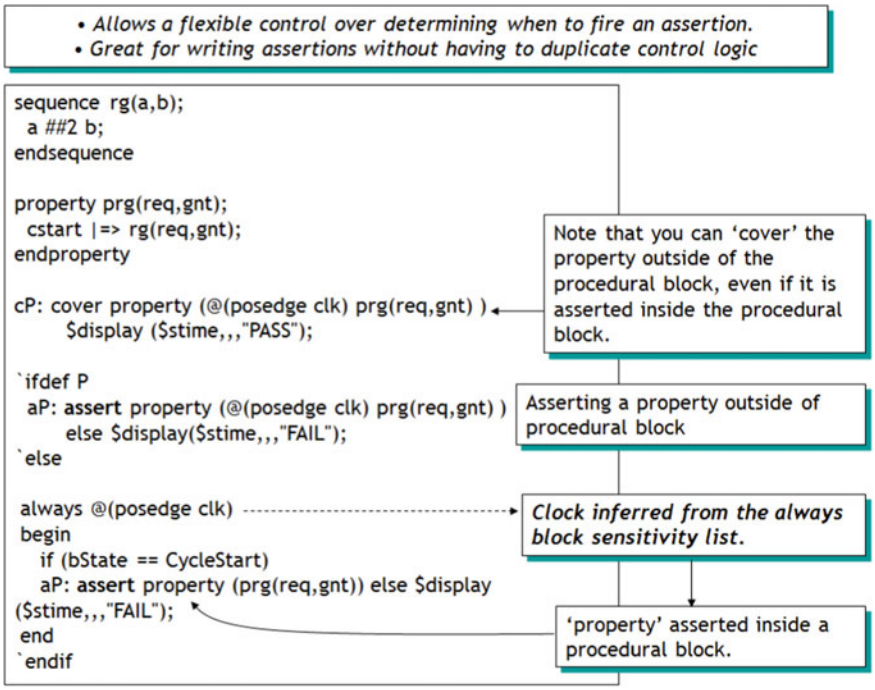


Fig. 14.1 Embedding concurrent assertions in procedural code

Yep, you can indeed assert a property (i.e. concurrent property) from a procedural block. Note that property and sequence itself are declared outside of the procedural block.

Off the bat, what is the difference than between immediate assertion and embedding a concurrent assertion in the procedural block? Well, immediate assertion is 'assert' and not 'assert property' and it is non-temporal domain 'assert'. In contrast, a concurrent assertion that is embedded in a procedural block is the regular concurrent assertion 'assert property' (i.e. it can be temporal). In other words, an immediate assertion embedded in the procedural code will complete in zero time, while the concurrent assertion may or may not finish in zero time. But is the concurrent assertion in the procedural code blocking or non-blocking? Hang on to this thought for a while.

To reiterate, the immediate assertion embedded in procedural code must complete in zero time. A concurrent assertion embedded in the procedural code may or may not finish in zero time.

Figure 14.1 points out that the 'condition' under which you want to fire an assertion is already modeled behaviorally and do not need to be duplicated in an assertion (as an antecedent). The example shows both ways of asserting a property. 'ifdef P shows the regular way of asserting the property that we have seen throughout this book. 'else shows the same property being asserted from an always block. But note that in the procedural block the assertion is preceded by 'if (bState == CycleStart) condition. In other words, a condition that could be already in the behavioral code is used to condition an assertion. If the property was 'asserted' outside of the procedural block (as we have done until now in the book) you would have to duplicate the condition in the procedural block as an antecedent in the property.

Let us turn our attention back to embedded concurrent assertion being blocking or non-blocking. What happens when you fire a concurrent assertion from the procedural code and it does not finish in zero time? What happens to the procedural code that follows the concurrent assertion? Will it stall until the concurrent assertion finishes (blocking)? Or will the following code continue to execute in parallel to the fired concurrent assertion (non-blocking)? That's what the Fig. 14.2 explains.

There are two properties 'pr1' and 'pr2'. They both 'consume' time, i.e. they advance time. The procedural block 'always @ (popsedge clk) asserts both these properties one after another without any time lapse between the two. How will this code execute? The procedural code will encounter 'assert property (pr1..)' and fire it. 'pr1' will start its evaluation by looking for cstart to be high and follow on through with the consequent. In other words, 'pr1' is waiting for something to happen in time domain. But the procedural code that fired it *won't* wait for 'pr1' to complete. It will move on to the very next statement which is 'assert property (pr2..)' and fire it as well. So, now you have 'pr1' that is already under execution and 'pr2' that is just fired both executing in parallel and the procedural code moves on to other code that sequentially follows.

In short, the concurrent assertion in procedural code is non-blocking.

As shown in the simulation log, at time 10, (@ posedge clk) we fire 'pr1'. At the *same* time (since the very next statement is 'assert property (pr2…)') we fire 'pr2'. At time 30, 'cstart==1' and 'aStrob==0'. This means the antecedent condition of both 'pr1' and 'pr2' have been met. At 50, 'Wenb==0' which completes the property 'pr2' and the property passes and as shown at time 50 in simulation log. Therefore, the first thing you notice here is that even though 'pr1' was fired first, 'pr2' finished first. In other words, since both properties were non-blocking and executing on their own parallel threads, there is no temporal relationship between them or among 'pr1', 'pr2' and the procedural code. Following the same line of thought, see why both 'pr1' and 'pr2' pass at the same time at 90.

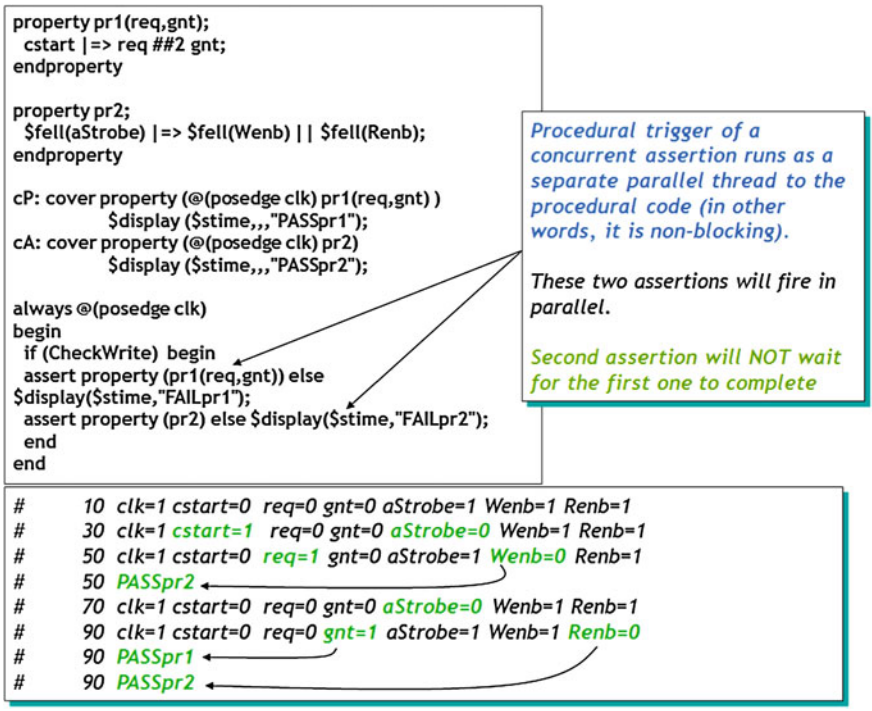


Fig. 14.2 Concurrent assertion embedded in procedural code is non-blocking

See the rules on inferring clock edge for the assertion in the procedural block. In addition, other nuances of semantic are noted in Fig. 14.3. In short, the clock inference for the embedded assertion comes from the 'always' block edge sensitivity. It is not derived from any other temporal domain condition (edge or level) that is embedded in the procedural code.

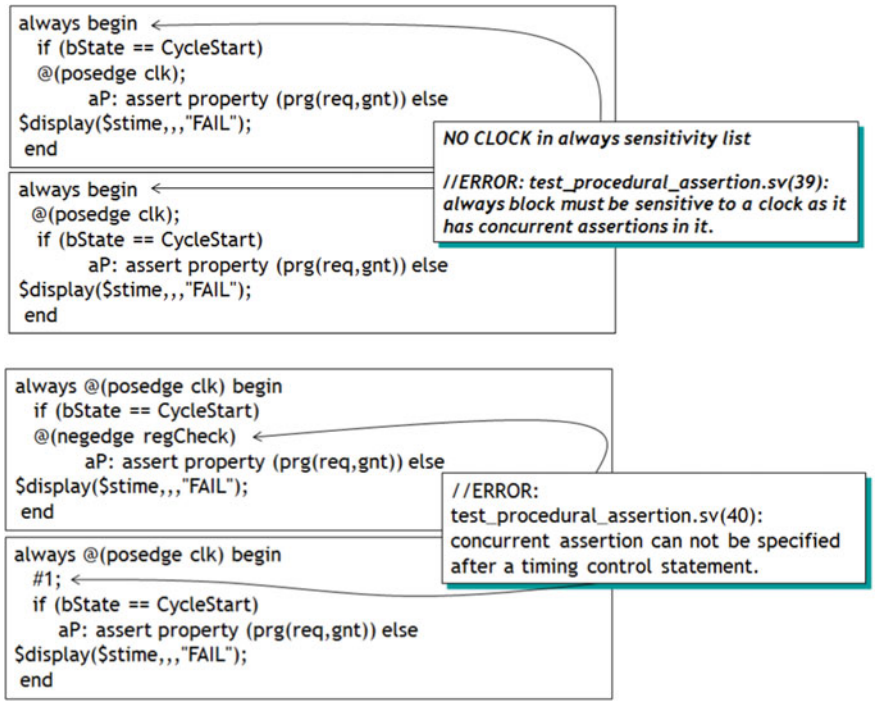


Fig. 14.3 Embedding concurrent assertions in procedural code—further nuances

14.3 Calling Subroutines

Attaching a subroutine to an expression is an excellent feature and a great boon to debugging effort and other applications. For example, if you'd like to know exactly when an expression is executed in a complex sequence (this is just but one example), you can 'attach' a Verilog task to the expression and display the conditions you are interested in Fig. 14.4 explains this scenario.

As shown in the figure, you can attach a subroutine to an expression, a sequence or to an expression or subsequence within a sequence. Note that the attached subroutine will execute on successful completion of either the expression or the sequence to which it is attached. For example, (not(cde,tdisp1)) in the topmost example of Fig. 14.4 means that 'tdisp1' will execute when 'cde' reaches its true conclusion. Else, it won't execute.

Figure 14.5 further explains when a subroutine is executed. First, at the top of the figure you notice that we 'attach' a local variable as well as a subroutine ($display task). Since $rose(ptrue) is the sequence to which the subroutine is attached, it will execute only when $rose(ptrue) is true. Similarly, the next part of the figure shows (pout == (local_data + 5), $display (…)), where (pout == (local_data + 5)) is the expression to which the $display subroutine is attached. Again, the subroutine $display will execute only if (pout == (local_data + 5)) is true.

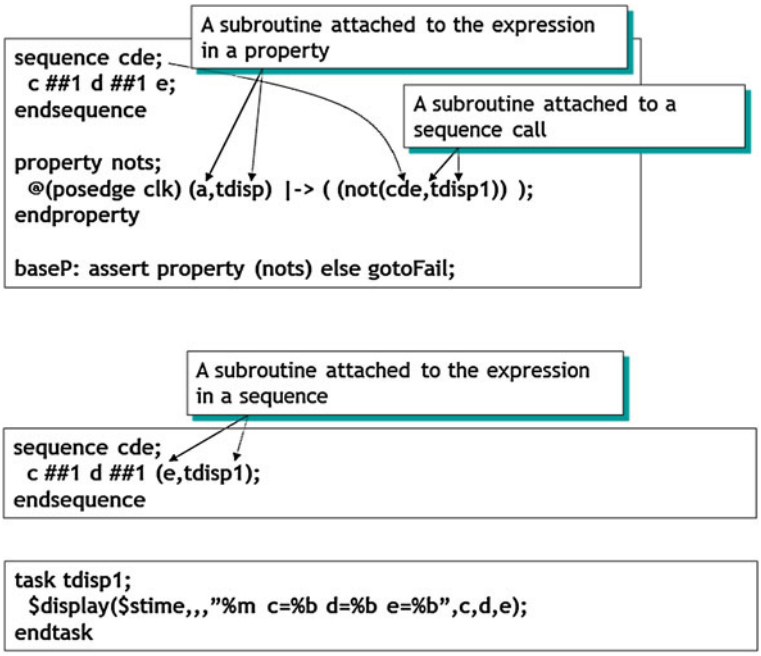


Fig. 14.4 Calling subroutines

You will also notice that $display in this figure (for most part) displays local variables. This is one of the important use of $display as a subroutine because local variables cannot be accessed from an action block (pass or fail).

```
sequence lvar_seq(pin,pout);
  int local_data;
  ($rose(ptrue),local_data = pin,$display($stime,,,"pin=%0d",pin) )
//                                 ^^^^^^^^^^^^^^^^^^^^^^^^^^^^^
//            This will be executed when $rose(ptrue) is detected..
   ##5
  (pout == (local_data+5),$display($stime,,,"pout=%0d",pout) );
//                          ^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^
//                          This will be executed ONLY IF
//                          the sequence MATCHES.
endsequence

property lvar;
  @(posedge clk) cStart |-> lvar_seq(pipe_in,pipe_out);
endproperty
```

Fig. 14.5 Calling subroutines—further nuances

In Fig. 14.6, the subroutine is a Verilog 'task'—lvar_seq_trigger which in turn contains a $display. But *I don't want you to run away with the idea that the only subroutine you can attach is the one that $displays something!* You can use a

subroutine to (e.g.) collect coverage information (using covergroups and coverpoints). We will see this with an example when we discuss Functional Coverage. *Since the attached subroutine can be task, you can think of many possible applications.*

```
sequence lvar_seq(pin,pout);
  int local_data;
  ($rose(ptrue),local_data = pin,lvar_seq_trigger(local_data))
   ##5
  (pout == (local_data+5),lvar_seq_match(pin,pout,local_data));
endsequence

property lvar;
  @(posedge clk) ptrue |-> lvar_seq(pipe_in,pipe_out);
endproperty

baseP: assert property (lvar) else gotoFail;
coverP: cover property (lvar) gotoPass;

task lvar_seq_trigger;
input ldata;
  $display($stime,,,"%m ldata=%0d",ldata);

  //$display($stime,,,"%m ldata=%0d",lvar_seq.pin);
  // ** Error: Hierarchical access to formal parameter pin' of 'lvar_seq' is illegal.
endtask

task lvar_seq_match;
input tpin,tpout,ldata;
  $display($stime,,,"%m pin=%0d pout=%0d ldata=%0d",tpin,tpout,ldata);
endtask
```

Fig. 14.6 Calling subroutines and local variables—application

The idea behind attaching a 'task' to the expression is that you can do whatever that Verilog allows you to do in a 'task' except that you cannot access the local variables of the sequence that invoked the 'task'. But you can indeed pass a local variable as an argument to the 'task' as shown in Fig. 14.6.

'sequence lvar_seq' has a local variable called 'local_data'. This local variable is passed to 'lvar_seq_trigger' as an actual argument. 'task lvar_seq_trigger' in turn uses that as an input 'ldata' and displays it. This is one way you can pass a local variable to the attached subroutine.

But note that you cannot access a variable (local or not) hierarchically from the attached subroutine (for example, task lvar_seq_trigger). This is shown with an ERROR in the figure. Here we tried to hierarchically access variable 'pin' in 'sequence lvar_seq' by using 'lvar_seq.pin'. That is a violation.

Note that the assertion from which you invoked the subroutine does not wait for completion of the subroutine or get any value back from the subroutine.

Finally, arguments passed to a subroutine must be by value or by reference ('ref' or 'const ref').

14.4 Sequence as a Formal Argument

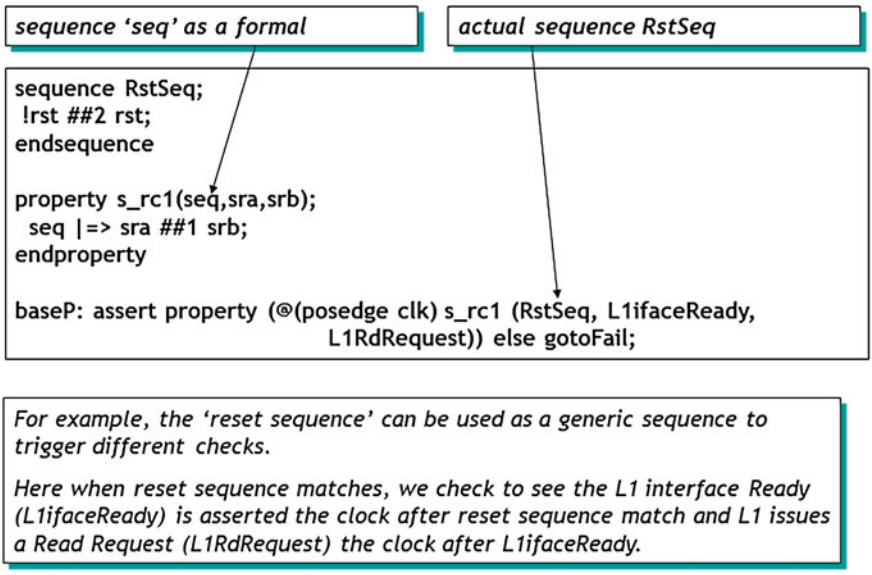


Fig. 14.7 Sequence as a formal argument

SystemVerilog assertions are indeed powerful as evident from this feature. You can send an entire sequence as an actual argument to a property or another sequence. One obvious advantage is that you may reuse a sequence in different properties as an actual to the property's formal argument. One example of this is the Reset Sequence as shown in Fig. 14.7. Reset sequence is often used in different properties as an antecedent. Write it once and pass it to different properties as an actual argument. That is Reusability with observability and debuggability. The sequence that is passed to a property can (obviously) be used on both the antecedent and consequent side.

14.5 Sequence as an Antecedent

Since a sequence can be passed as an actual argument there are many advantages. We saw one in Fig. 14.7. Here's another. Here, we define a simple sequence 'seq' and pass it to property 's_rc1'. In this property, we use 'seq' (i.e. c_seq in the property) as an antecedent (Fig. 14.8).

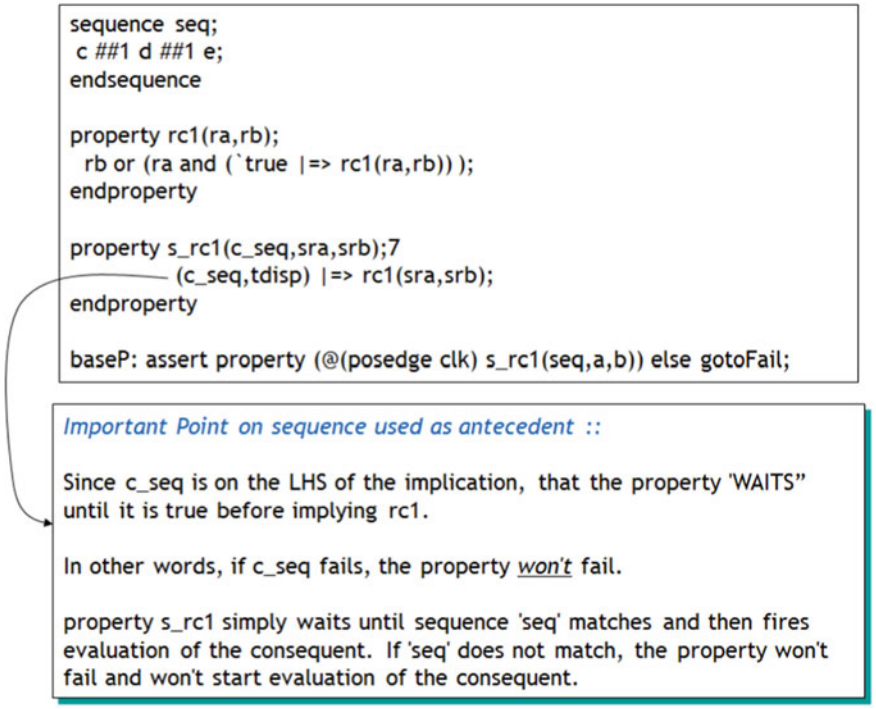


Fig. 14.8 Sequence as an antecedent

As with any antecedent, the property will wait for antecedent to be true and then imply the consequent. Now, with many operators (e.g. 'throughout') we have observed that the LHS and RHS of the operator is equally responsible for failure. If either side fails that the operator and hence the sequence/property fails. Important thing to note here is that in the cases of 'throughout' the operator was used in the consequent and not in antecedent. Anything that fails in consequent causes the property to fail. Here, a sequence is used in 'antecedent' meaning even if the sequence in antecedent fails, the property will not fail. Instead, the property will simply wait for the sequence 'c_seq' to be eventually be true only after which it will execute the consequent. This makes sense because consequent fires only when antecedent is sampled to be true.

Short end of the story is that no matter what you have in the antecedent, it will not cause a failure. Antecedent's job is to evaluate its expression/sequence and on sampling it to be true, imply the consequent.

14.6 Sequence in Sensitivity List

```
sequence sr1;
          @(posedge clk) req ##2 gnt;
endsequence

always @(sr1)
  $display($stime,,,"req ##2 gnt PASS");
```

Using sequence as an event trigger for always block.

Triggers only when the sequence matches.

```
# run -all
#       5  clk=1 req=0 gnt=0
#      15  clk=1 req=1 gnt=0
#      25  clk=1 req=0 gnt=0
#      35  clk=1 req=0 gnt=1
#      35  req ##2 gnt PASS

#      45  clk=1 req=1 gnt=0
#      55  clk=1 req=0 gnt=0
#      65  clk=1 req=0 gnt=0

#      75  clk=1 req=1 gnt=0
#      85  clk=1 req=0 gnt=0
#      95  clk=1 req=0 gnt=1
#      95  req ##2 gnt PASS
```

Fig. 14.9 Sequence in procedural block sensitivity list

Let us take the use of a 'sequence' even further. Guess what? You can use a sequence for event control either in the sensitivity list or as an explicit edge sensitive control in an initial block. You can use this feature very effectively because designing a temporal domain condition in SVA is far easier than using behavioral Verilog. You can design certain condition as a sequence and then use it in your procedural behavioral Verilog code as shown in Figs. 14.9 and 14.10.

Figure 14.9 shows that the 'always' block waits for sequence 'sr1' to complete and simply display its PASS result. Can you figure out why there is no FAIL report? Was "always @ (sr1)" triggered when 'gnt' did not follow 'req' after 2 clocks? Please experiment and see what happens.

The sequence in Fig. 14.10 says that @ (posedge clk) if $rose(read) is sampled high (edge) that there should be at least 1 readC (read complete). The 'initial' block waits for this sequence to complete (using @ (ReadComplete) and then issues the next Read.

As you can see, this feature is extremely powerful in using the power of sequence in designing your SystemVerilog test-bench code.

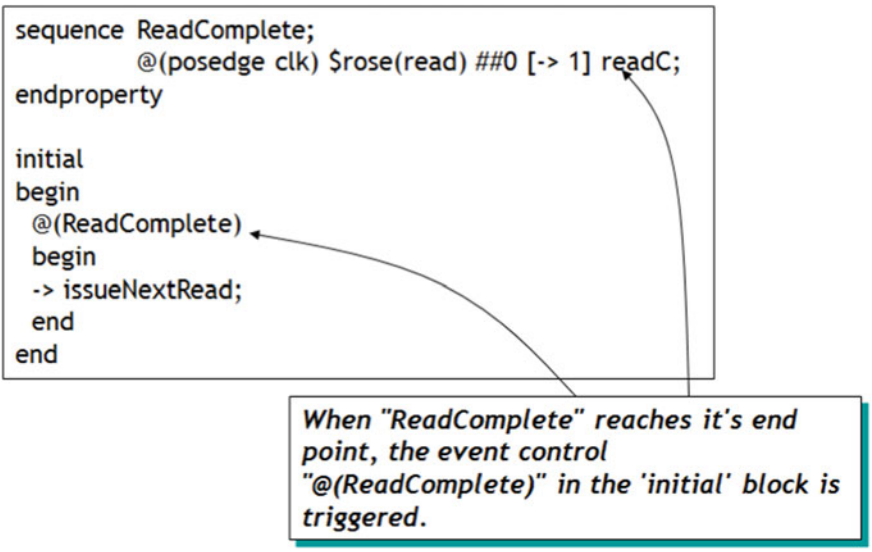


Fig. 14.10 Sequence in 'sensitivity' list

14.7 Building a Counter

Following is an example of how to build a counter using the consecutive repetition operator [m]*

```
property checkCounter;
int LCount;
 @(posedge clk) disable iff (!rst_n)

        (
                ($rose(startCount), LCount=initCount ) ##1

                (1, LCount = LCount+1)[*0:$] ##1 (LCount == maxCount) |->

                (Intr == 1'b1)
        );
endproperty
assert property (checkCounter);
```

Fig. 14.11 Building a counter using local variables

Ok, that is enough of sequences (for a while, at least). Let us see how we can effectively use local variables and the consecutive repetition operator to build something!

Let us build a counter. Why? There are many applications where you will be able to use this example. For example you want to make sure that an incoming

packet on a network generates an interrupt when it's payload reaches a maximum threshold (count).

The property checkCounter declares a local 'int' called 'LCount'. It waits for a rising edge on 'startCount' and on this rising edge, it stores 'initCount' into 'LCount' (initCount is defined elsewhere in your procedural code).

It then waits for 1 clock and increments LCount by 1 and continues to do so at every clock until LCount reaches maxCount. The consecutive repetition operator [*0:$] does the counting. In other words, "LCount = LCount + 1" repeats at every posedge clk until you reach "LCount == maxCount". Once the maxCount is reached, the antecedent implies at the same clock (overlapping implication) that the intr be asserted.

Quick Note: In this book, as you have noticed, instead of giving large applications and then describe a limited set of SVA features, I have chosen to describe each operator with simple applications so that you clearly understand the workings of the operator and apply the operator features to design your assertions.

14.8 Clock Delay: What if You Want *Variable* Clock Delay?

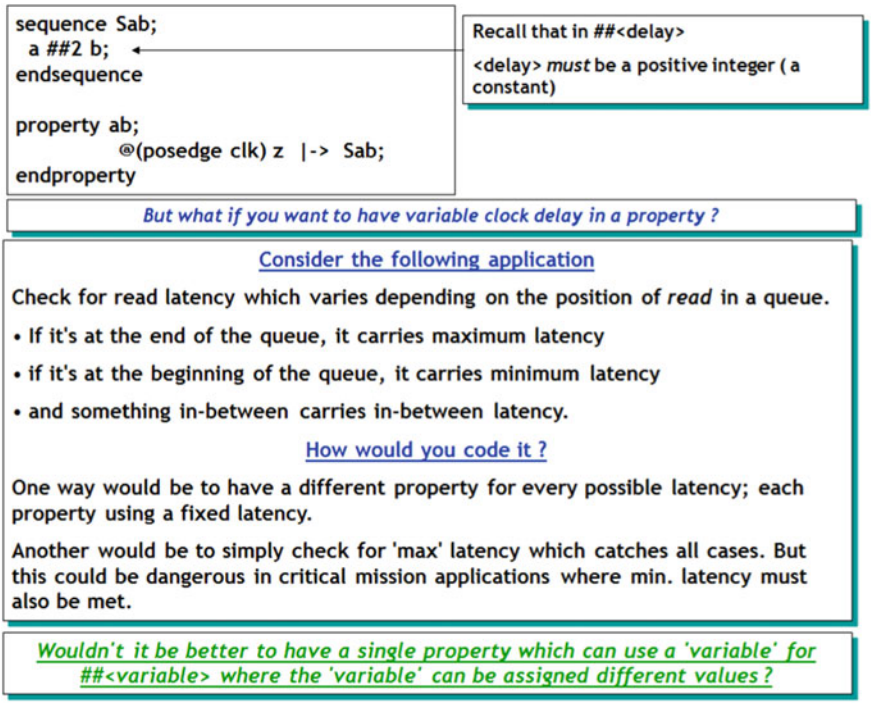


Fig. 14.12 Variable delay—problem statement

Figure 14.11 built a counter which can be used to create a variable delay model. Note that SVA allows only constant fixed delays with its delay operator. So, the example in Figs. 14.12 and 14.13 demonstrates a strategy to get around this limitation.

Figure 14.12 describes a typical specification. We need to check for variable latency based on the position of a 'read' in the read queue. In other words, if the 'read' is at the end of the queue, 'read' will complete with maximum latency. On the contrary if it's at the beginning of the queue, it will complete with minimum latency. Or with a latency anywhere in the middle.

Since the delay (or range delay) operator does not allow variable delay, how would you model this with one generic assertion? You do not want to create a separate assertion for each of the fixed latency. That is the problem statement. Now let us see how we solve this. Consider this example as an idea generator.

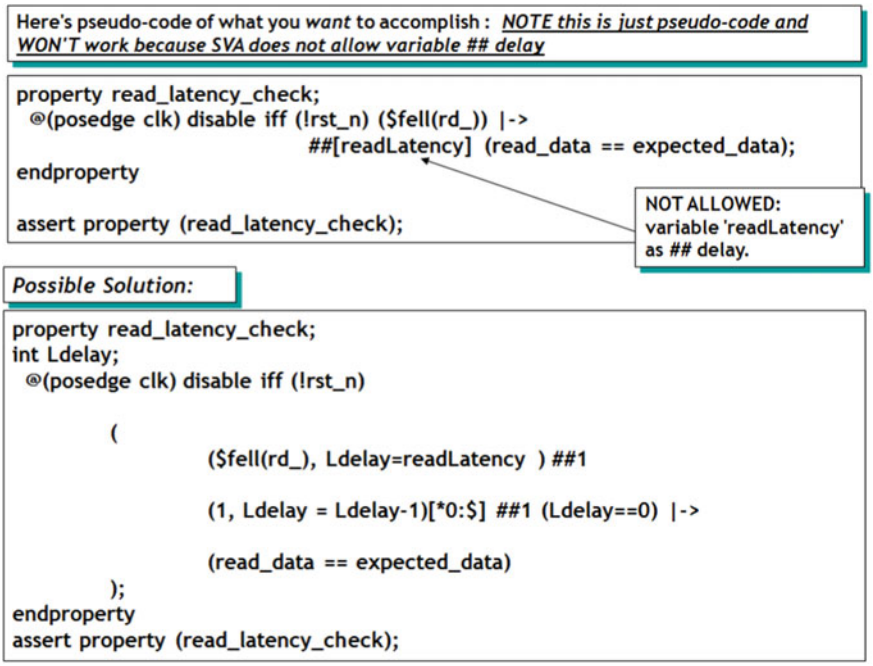


Fig. 14.13 Variable delay—solution

The concept in Fig. 14.13 is identical to building a counter example. Here instead of incrementing the local variable we decrement it until it reaches zero. In this application readLatency is defined in your procedural code and it changes based on the position of Read in the read queue. That part of the code is not shown here.

When the property 'read_latecncy_check' is asserted, it will assign the read-Latency to Ldelay on assertion ($fell(rd_)) and decrement it at every posedge clk, until it reaches 0.

(1, Ldelay = Ldelay-1)[*0:$] ##1 (Ldelay==0)

Ldelay is decremented consecutively at every posedge clk until Ldelay==0. Need for '1' in (1, Ldelay = Ldelay-1)? Why? Recall that we can assign to a local variable when that assignment is attached to an expression. Since we do not have any explicit expression, we simply use 'always true' as an expression.

You can continue to change readLatency from procedural code based on the position of 'read' in your read queue and use the same property to check for different latencies of read in the read queue.

This simple example has very powerful application capabilities.

14.9 What if the 'action block' is Blocking?

We have seen that the assertion of a property ("assert property") allows you two 'action' blocks. One is triggered when the property passes and the other when it fails.

This action block can contain any procedural code that SystemVerilog supports. The procedural block can have temporal domain 'delay' (e.g. @ (posedge cc) or 'wait sig', etc.). That is when you need to carefully weigh in the consequences. If there is no 'delay' in the block, life is straightforward. The "assert property" triggers the block without any delay; the block executes in 0 time; returns and the property moves along with its execution. But if there are delays in the action block, here's what happens.

The property at top left of Fig. 14.14 says "assert property (pr1) else failtask". If the property fails, call a task called 'failtask'. 'failtask' in turn waits for 4 @ (posedge clk) and returns from the task. The 4 clock delay is just an example for temporal delay.

Now let us look at the simulation log. At time 30, req=1, so the property pr1 moves along. At time 70, gnt=0 which is a failure condition because gnt should have been '1' at that time. Since there is a failure, the 'failtask' is invoked at time 70 (the time of failure). The 'failtask' waits for 4 posedge clks, which are displayed in the log file at time 90, 110, 130, 150. While the 'failtask' was waiting for its clocks to complete, at time 110, req goes high again. So, the property starts executing and expects 'gnt' to be high at 150. And again gnt is '0', so the property should fail. But it does not!! Why? Because at time 150, the 'failtask' was still completing its 4th clock wait. Since the 4th clock wasn't over by the time the 'gnt' based failure came along at 150, the failure got suppressed because first invocation of 'failtask' wasn't over.

The point is, if you call a procedural block that does not complete in '0' time, and if the next trigger of the property antecedent comes along causing another

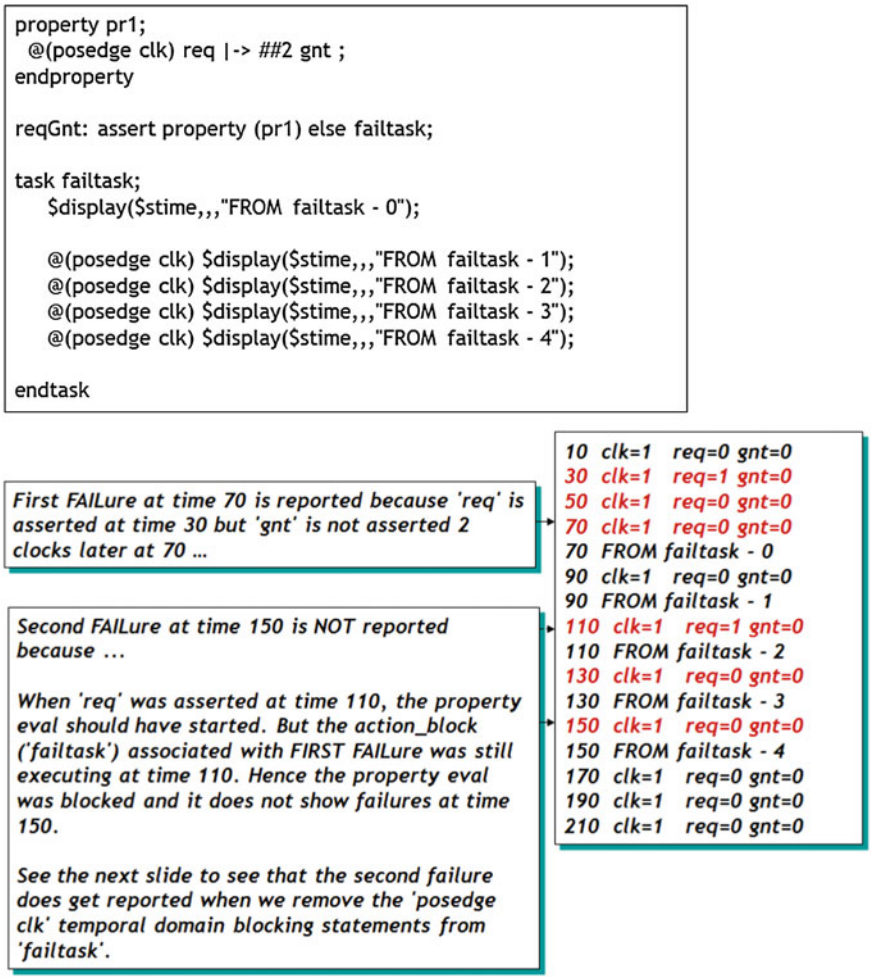


Fig. 14.14 Blocking action block

pass/fail, the next trigger of the action block associated with pass/fail won't happen. So, be careful in using time lapse in your action block(s).

Figure 14.15 simulation logs highlight the same point. There is one example with time lapse in the action block and another without.

As shown in Fig. 14.15, the properties on LHS and RHS are identical, except that LHS action block calls a 'failtask' that elapses time (4 clocks). The RHS on the other hand calls 'failtask' that does not elapse any time.

The 'req' condition is also identical in both simulation logs. But the RHS shows two invocations of 'FROM failtask - 0' while the LHS log shows only one invocation (as explained above for Fig. 14.14) because the action block is 'blocking' and does not allow reentry into an already executing action block.

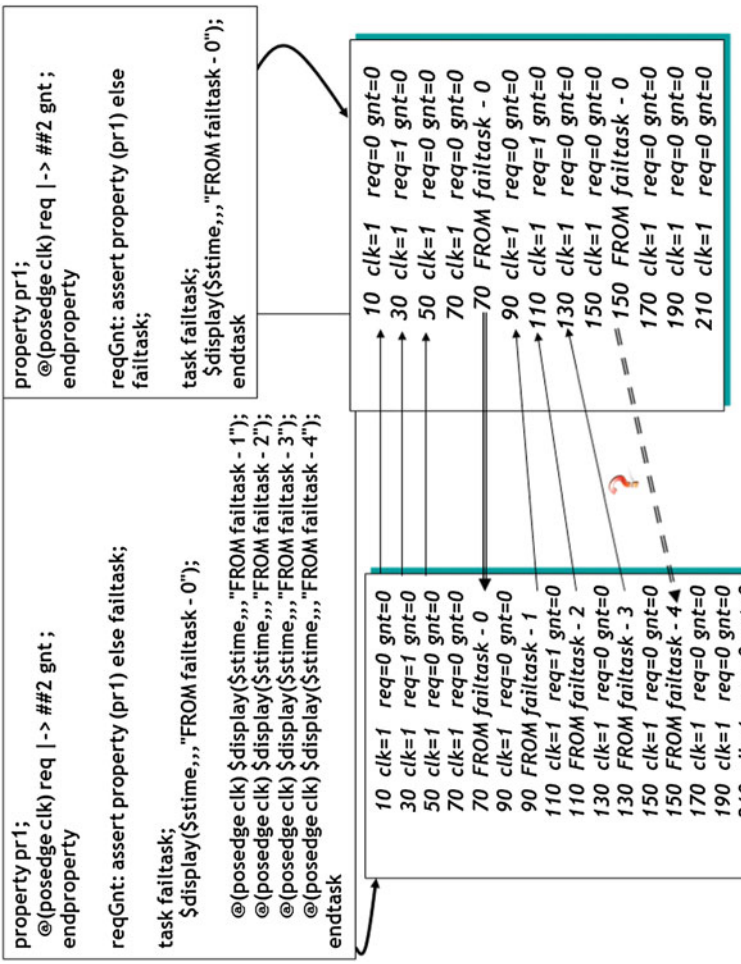


Fig. 14.15 Blocking versus non-blocking action block

14.10 Interesting Observation with Multiple Implications in a Property. Be Very Careful…

Can you have multiple implications in a property? Sure you can. However, you need to very carefully understand the implications of multiple implications (that sounds funny) in a property. Let us look an example and understand how this works.

In Fig. 14.16, the property mclocks (at first glance) looks very benign. But play close attention and you will see two implications. @ (posedge clk) if 'a' is true that implies "'bSeq' ##1 c", which implies 'dSeq'. One antecedent implies a consequent which acts as the antecedent for another consequent.

Now, let us look at the simulation log. At time 175, a=1, so the property starts evaluation and implies "bSeq ##1 c". At time 185 'bSeq' matches, so the property now looks for ##1 c. At time 195, c is –not- equal to '1' but the property does not

```
sequence bSeq;
 ##[1:5] b;
endsequence

sequence dSeq;
 ##2 d ##2 e;
endsequence

property mclocks;
  @(posedge clk) a |-> bSeq ##1 c |-> dSeq;
endproperty
```

```
#      165  CLK # 17 :: clk=1 a=0 b=0 c=0 d=0 e=1
#      175  CLK # 18 :: clk=1 a=1 b=0 c=1 d=0 e=0 //a=1 so start
#      185  CLK # 19 :: clk=1 a=0 b=1 c=0 d=0 e=0
                        //b=1 next clock; so 'bSeq' matches

#      195  CLK # 20 :: clk=1 a=0 b=0 c=0 d=0 e=0
                        //But c NE 1 the next clock
                        //and the property does NOT fail.

#      205  CLK # 21 :: clk=1 a=0 b=0 c=0 d=0 e=0
#      215  CLK # 22 :: clk=1 a=0 b=0 c=1 d=0 e=0

//So, when 'c' does go '1' a couple of clocks later, the 'dSeq' seq
//won't start eval at that time. The fact that 'c' did not go '1'
//the very next clock after 'bSeq' matches that the entire
//property will simply not get evaluated for pass or fail; until //'a' is asserted
again.

#      225  CLK # 23 :: clk=1 a=0 b=0 c=0 d=0 e=0
#      235  CLK # 24 :: clk=1 a=0 b=0 c=0 d=1 e=0
#      245  CLK # 25 :: clk=1 a=0 b=0 c=0 d=0 e=0
#      255  CLK # 26 :: clk=1 a=0 b=0 c=0 d=0 e=1
#      265  CLK # 27 :: clk=1 a=0 b=0 c=0 d=0 e=1
```

Fig. 14.16 Multiple implications in a property

fail. Wow! Reason? Note that 'bSeq ##1 c' is now an antecedent for 'dSeq' and as we know if there is no match on antecedent that the consequent won't be evaluated and the property won't fail. Here that seems to apply even though 'bSeq ## 1' is a consequent, it is also an antecedent. Language anomaly? Not really, but the behavior of such properties is not quite intuitive. Since 'bSeq ##1 c' did not match, the entire property is discarded and the property again waits for "a==1" to start all over again.

Confusing? Well, it is. Hence, please don't use such multiple implication properties unless you are absolutely sure that that's what you want. I've seen engineers use it because the logic seems intuitive, but the behavior is not.

14.11 Subsequence in a Sequence

A sequence can be embedded in another sequence. The embedded sequence can be called a subsequence. Figure 14.17 shows that sequence 'abc' is embedded into sequence 'abcRule'. The embedded subsequence infers the clock from the parent sequence, if the subsequence does not have an explicit clock of its own.

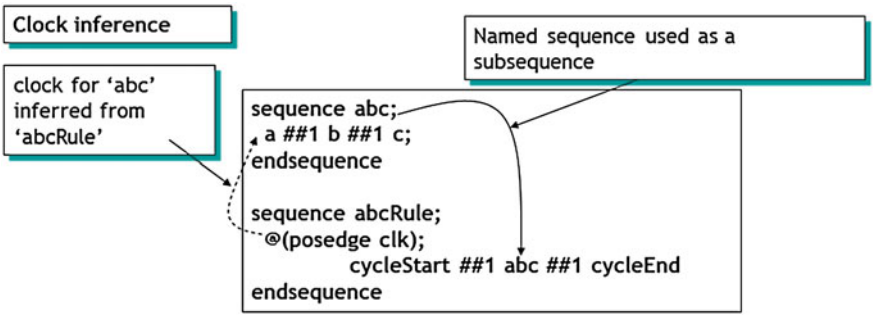


Fig. 14.17 Subsequence in a sequence—clock inference

Also, as shown in Fig. 14.18, a sequence can be used both as an antecedent and/or a consequent.

As shown, the antecedent is sequence 's1', which implies sequence 's2' as consequent. Here, each sequence has its own explicit clock. However, if that were not the case, the subsequences would inherit (inference) the clock from property s1tos2.

The reason for pointing out this usage is, again, to emphasize that it's best to break down a property into smaller sequences and then build the larger overall property. The smaller the sequence, the better it is for debuggability and controllability.

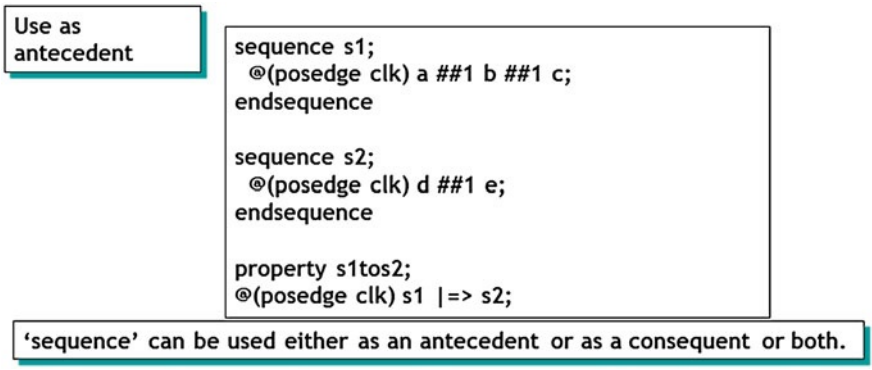


Fig. 14.18 Subsequence in a sequence

14.12 Cyclic Dependency

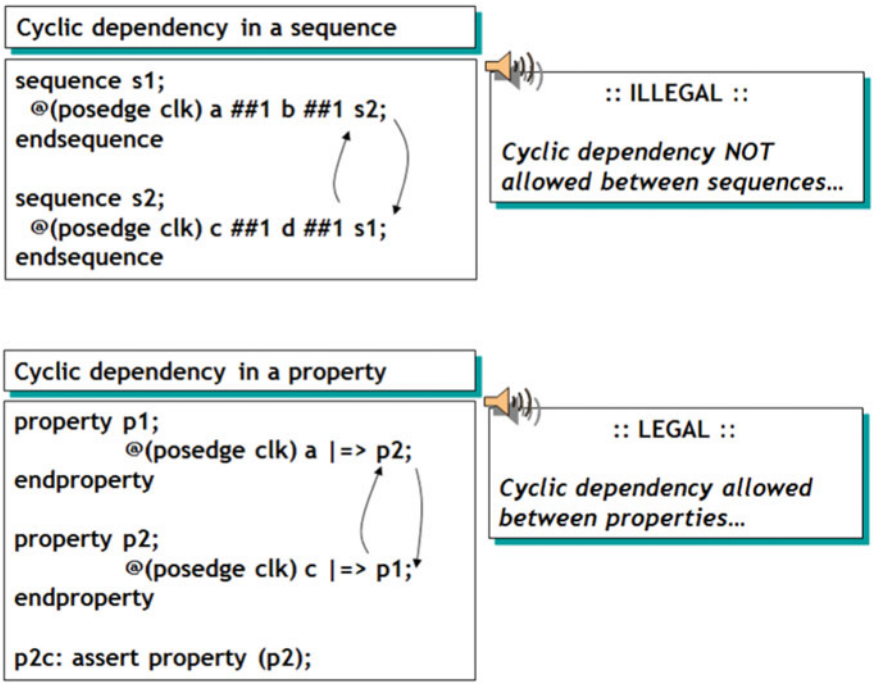


Fig. 14.19 Cyclic dependency

As shown in Fig. 14.19, you can indeed have cyclic dependency between properties but *not* among sequences. But *note that the cyclic dependency between properties is only between consequent of the property, not the antecedent*.

What is the use of this feature? If you want to check for continuous toggle between two states of a state machine, you can use this property. The property as shown in this example will never complete until simulation ends.

Note also that you cannot do something like "c |=> d ##1 e ##1 p1". You cannot use another property as a subsequence for cyclic dependency. You will get the following Error.

** Error: massert.v(42): Illegal SVA property value in RHS of '##' expression.

14.13 Refinement on a Theme…

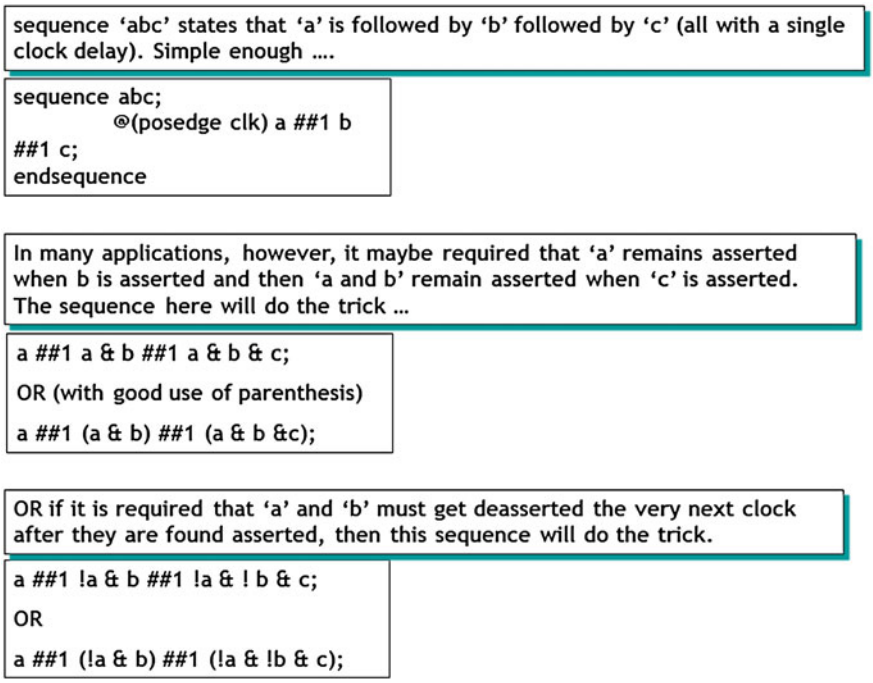


Fig. 14.20 Refinements on a theme

14.14 Simulation Performance Efficiency

In Fig. 14.21, the top property rdyProtocol says that if rdy is true then you must get a rdyAck. We have designed that using the constant delay range. Nothing wrong with that, but (as seen from simulation results), the infinite range based design runs slower than the one that does not use such a range. This by no means prohibit use of ##[1:$], but if you can find a better way to solve the problem, you will get better

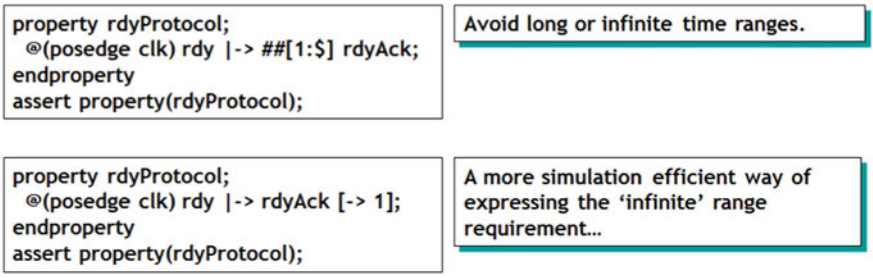


Fig. 14.21 Simulation performance efficiency

simulation efficiency. The bottom part of Fig. 14.21 shows the alternate way. It uses the 'goto' operator, which models the same behavior, namely, that there will be at least 1 rdyAck after a rdy.

14.15 It's a Vacuous World! Huh?

This section could have gone much earlier in the book but I did not want the reader to get confused from the get go. Once you go through this example, you will see why the 'implication' operator is (almost) a must in an assertion. The example figures below have detailed annotation for ease of understanding. Hence they are not followed by a lot of text.

Here we go.

14.15.1 Concurrent Assertion –Without- an Implication

Let us examine Fig. 14.22.

There is no implication operator in property pr1. As Fig. 14.22 shows, property 'pr1' reads as "@ (posedge clk) req should be true and 2 clocks later gnt should be true". Note that we have not used implication operator in the property. Hence, read the property carefully. It does –not- say that "*if*" req is true that the property should check for gnt. It simply says that 'req' be true at the posedge clk and 2 clks later gnt be true. Hence, every clock that req is *not* true the property FAILs. Is that what we really want? I don't think so. That's where an implication operator comes into picture.

More important, do you notice that at time 90, the property PASSes as well as FAILs !! Amazing! The property passes because at time 50, req=1 so the property looks for gnt=1 at 90. It does find gnt=1 at 90, so it PASSes. But since req=0 at 90, it also FAILs. Amazing, again!

My suggestion, do NOT use properties without implication, unless you are absolutely sure of what you are doing. Read On. The story does not quite end with implication either… but there is hope.

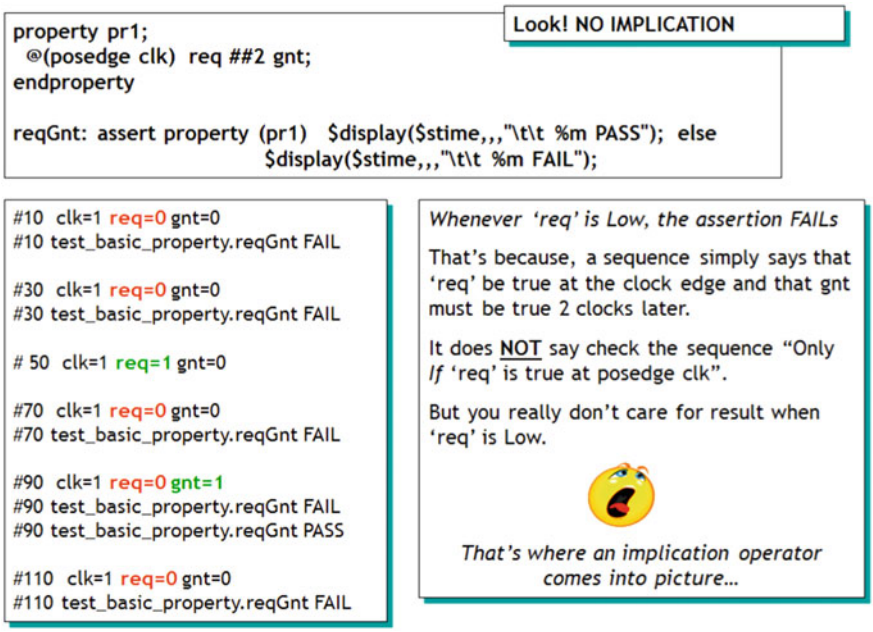


Fig. 14.22 Assertion without implication operator

14.15.2 Concurrent Assertion –with- an Implication

Ok, so we decide to add an implication operator as in "@ (posedge clk) req |- > ##2 gnt;" so that we don't get false failures. But wait! See the simulation log in Fig. 14.23 carefully. Now the assertion passes whenever req=0. What's going on?

Everything seems Ok. If the antecedent is not true, the consequent won't fire. But when the antecedent is not true, the properties PASS action block triggers and tells us that the property PASSes. Read on.

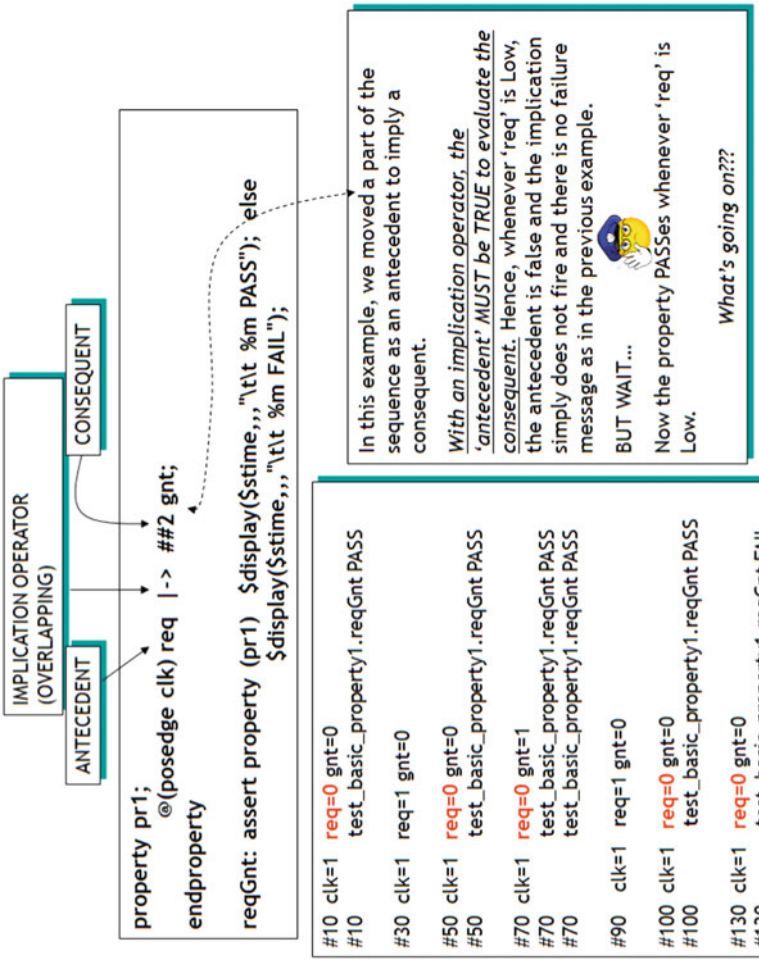
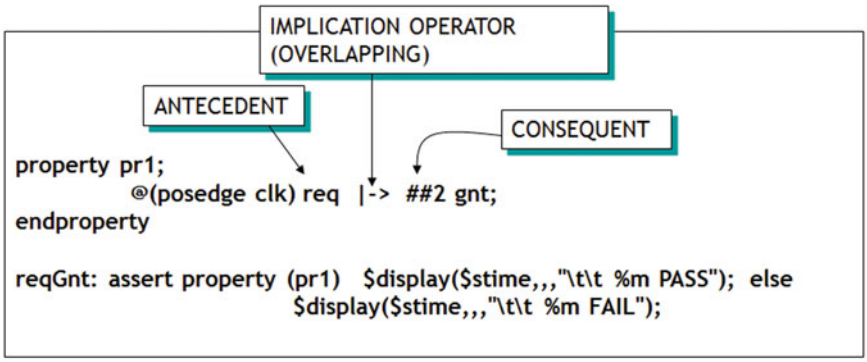


Fig. 14.23 Assertion resulting in vacuous pass

14.15.3 Vacuous Pass. What?



LRM 3.1a (Page 232) ::

"If there is no match of the antecedent sequence_expr, then evaluation of the implication succeeds vacuously and returns true"

A couple of ways to get around this...

One is to simply not use the action_block associated with 'pass' (duh...) of the property, so that you don't get pass indication vacuously

But what if you do want to know when the property passes...

The reason we get a PASS on the antecedent failure is that according to the LRM "If there is no match of the antecedent sequence_expr, then evaluation of the implication succeeds vacuously and returns true". Hence, whenever you see 'req' low, you get a 'vacuous' pass which triggers the PASS action block and we get the PASS display.

Ok, so what is the solution? Why did not we see this behavior until now with all the examples we have been through? Read on…

14.15.4 Concurrent Assertion–with 'cover'

There are two ways to overcome this behavior that we do not want. One is to simply ignore the PASS action block on 'assert' of a property, i.e. simply do not have a PASS action block. That way if there is a vacuous pass, our log will not be cluttered with misleading PASS messages. Note that ignoring the so-called vacuous pass is harmless. This is the obvious solution.

But what if you do want to know when the property PASSes? That's where 'cover' comes into picture.

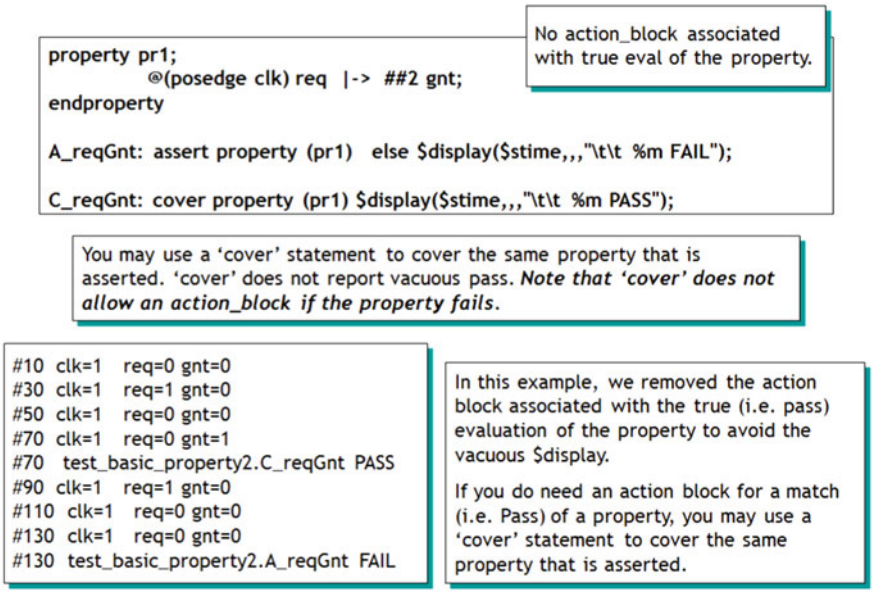


Fig. 14.24 Assertion with 'cover' for PASS

The solution with 'cover' allows us to see if the property is indeed covered (i.e. exercised). 'cover' does *not* have the vacuous pass property. It indicates at the *end* of the assertion if it has been covered. When it is covered, it triggers a PASS action block. In this action block you may put a $display statement to indicate that the property has been covered or that it has 'passed'.

Note that 'cover' simply does *not* have a FAIL action block and does not have the vacuous pass property.

This way, with 'assert' and 'cover', we have a method to code an assertion that gives us the required FAIL and PASS indication without any other message. Please read the simulation log carefully in Fig. 14.24 to see the behavior of the property.

Note also the use of "%m" in the $display task. This good old Verilog feature displays the entire path to the assertion. This is one way to distinguish two properties with same name in two separate scopes.

14.16 Empty Sequence

In Fig. 14.25, we are using the consecutive operator '*' but with '0' repetition [*0]. In other words, we are saying 'b' should not repeat *ever*. In yet other words, that means 'b' simply does not exist (empty) even though it is part of the property. Hence, "b[*0] ##1 !a" simply means check for empty sequence 'b' and 1 clock

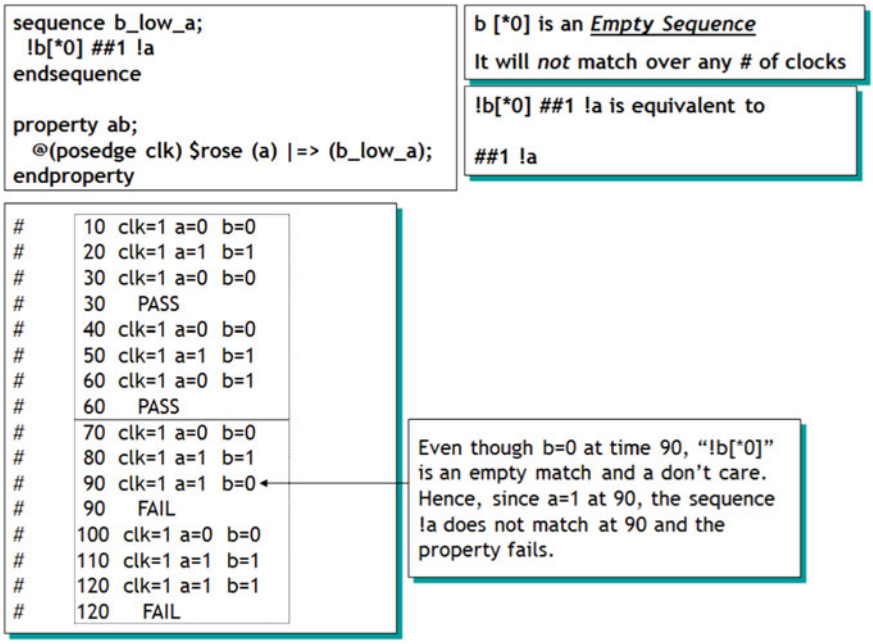


Fig. 14.25 Empty match [*m] where m=0

later check for '!a'. Since, empty sequence does not mean anything, we are basically checking for '!a '1 clock after $rose(a).

Following examples are given for the sake of completeness. Regard them as Reference Material.

Figure 14.26 is indeed interesting. LRM provides two rules on how to interpret (seq ##n *empty*) and (*empty* ##n seq) both with n > 0. The explanation is noted at the top of Fig. 14.26. To make that clear, let us go through the example.

Property 'ab' says that if the antecedent 'z' is true that the consequent sequence 'sc1' should execute. Sequence 'sc1' says that 'a' be true when 'z' is true; then (according to the LRM rule (seq ##n *empty* == seq##(n-1) 'true), the sequence can be read as 'a' be true; then 'b' may not be true (i.e. empty—does not exist) at all or will continue to repeat forever until c==1.

Let us look at the simulation log to see if the new definition holds.

At 30, z=1 so the property looks for 'a'=1 at the same time. 'a'=1 at 30. 'b' is also equal to '1'—which does not really matter because 'b' can have zero match, as long as there is c==1 at 1 clock after the *last* 'b' or 'a'. In our case which started at 30, we do have c==1 at 50 which is one clock after 'a==1' as well as 'b==1'. Hence the property passes.

At 70, z=1,a=1 but b=0. That's an empty match. Hence, the property looks for c==1 after the last 'a'. It finds that at 90 and the property passes.

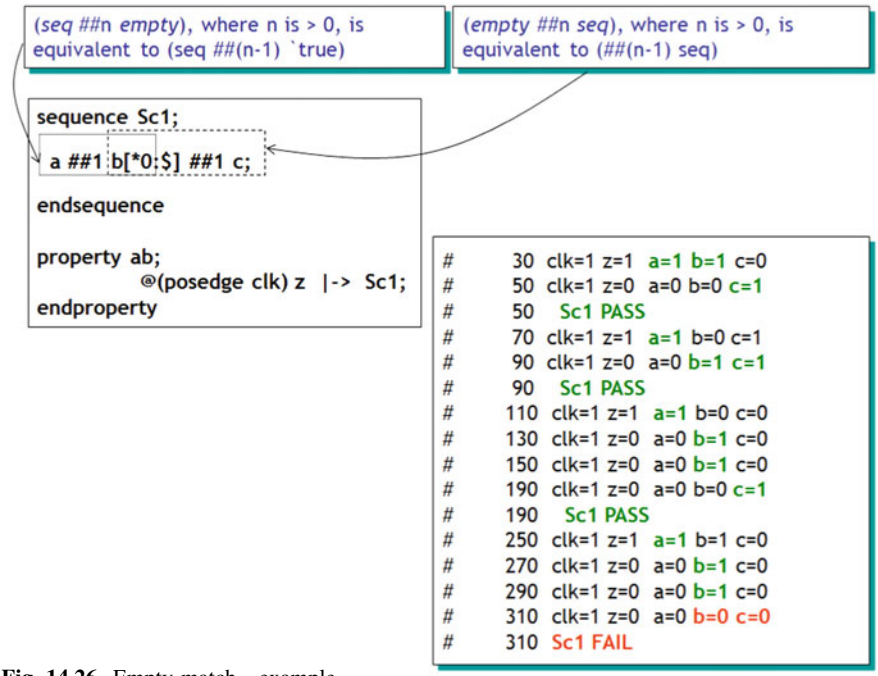


Fig. 14.26 Empty match—example

At 110, z=1, a=1, b=0. Next clock at 130, a=0 and c is also equal to '0'—but 'b'=1. As we saw before, 'b' may not match or may continually match forever until "c==1". Since c==0 at time 130, the property continues to look for b==1 until c==1. That happens at time 150 (b==1) and 190 (c==1) and the property passes.

At 250, z=1, a=1 and b=1. The next clock at 270, c is still zero, so the property continues to see that b remains '1'. At 290, b==1, so we move on. But at time 310, 'b' has not remained asserted and 'c' is not equal to '1' either. 'c' should have been '1' (to satisfy b[*0:$] ##1 c) –or- 'b' should have remain asserted. Neither happens and the property fails.

The example in Fig. 14.27 can be used effectively when you want to check that if a certain sequence takes place that another never takes place. You can do that with non-zero consecutive repetition operator also, but the [*0] or [= 0] makes it that much easier.

For example, in the following example,

@ (posedge clk) a | => b[= 0];

means that on 'a' being true, one clock later, 'b' should never occur. In other words, 'b' should be negated (zero) forever. This is quite straightforward to read/interpret. The behavior is shown in simulation log in Fig. 14.27.

So, how else would you write this property?

*@ (posedge clk) a | => !b[*1:$];*

Same meaning. Once ‘a’ is true that starting next clock ‘b’ should remain ‘!b’ consecutively forever.

```
property ab;
          @(posedge clk) a |=> b [=0];
endproperty
```

b [=0]

means that the signal ‘b’ should *never* be true (in other words, it means that the # of non-consecutive occurrences are ZERO).

```
#        5  clk=1 a=1 b=0
#       15  clk=1 a=0 b=0
#       15          property ab PASS

#       35  clk=1 a=1 b=0
#       45  clk=1 a=0 b=0
#       45          property ab PASS
#       55  clk=1 a=0 b=1

#       65  clk=1 a=1 b=0
#       75  clk=1 a=0 b=1
#       75          property ab FAIL
```

Fig. 14.27 Empty match example—II

Following is purely reference material. Keep it in your back pocket. It will be useful on a rainy day! (Fig. 14.28).

SystemVerilog 3.1a LRM; Page 210

(*empty ##0 seq*) does not result in a match

(*seq ##0 empty*) does not result in a match

(*empty ##n seq*), where n is > 0, is equivalent to (##(n-1) seq)

(*seq ##n empty*), where n is > 0, is equivalent to (seq ##(n-1) `true)

Examples:

b ##1 (a[*0] ##0 c) - will never produce a match

b ##1 a[*0:1] ##2 c is equivalent to
(b ##2 c) or (b ##1 a ##2 c)

Fig. 14.28 Empty sequence. Further rules

Chapter 15
Asynchronous Assertions !!!

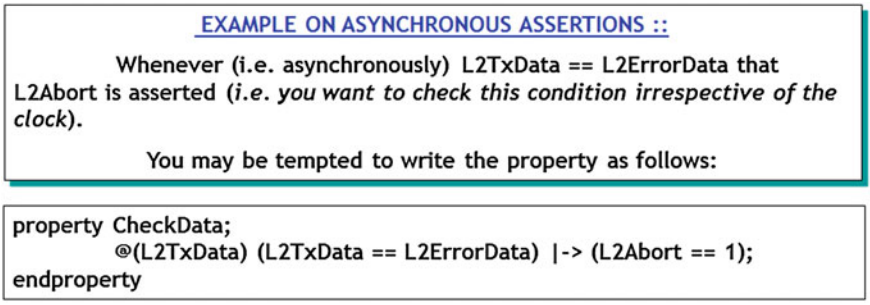


Fig. 15.1 Asynchronous assertion—problem statement

So far in the book we have always used a synchronous clock edge as the sampling edge for the assertion. That is for good reason. The example presented here uses an asynchronous edge (perfectly legal) as the sampling edge. The problem statement goes something like "whenever (i.e. asynchronously) L2TxData == L2ErrorData that L2Abort is asserted". Now that looks very logical to implement without the need for a clock. So, we write a property as shown in the Fig. 15.1. We simply say that @ (L2TxData) (i.e. whenever L2TxData changes) that we compare L2TxData == L2ErrorData and if that matches we imply that L2Abort ==1.

A. B. Mehta, *SystemVerilog Assertions and Functional Coverage*,
DOI: 10.1007/978-1-4614-7324-4_15,

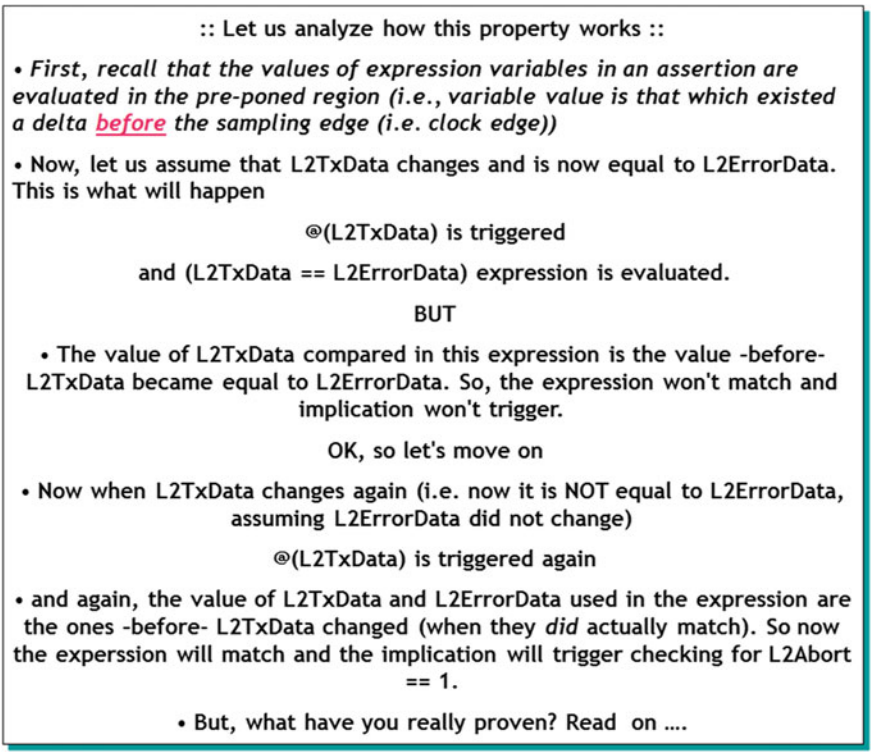


Fig. 15.1 (continued)

This sounds very logical. What is wrong with it? Hmm… many things. The annotation in Fig. 15.1 takes you systematically on what is going on. Please study it carefully to see why there is a problem. We will not repeat that explanation of the figure again. But here's the high level hint on the problem. The 'sampling edge' (namely, @ (L2TxData)) is also used in the comparison expression. Since the value of variables in an expression are always evaluated in the preponed region that the value of L2TxData in the expression won't be the same as when @ (L2TxData) changed. If this sounds confusing, well it is. That is the reason I do not recommend asynchronous assertions.

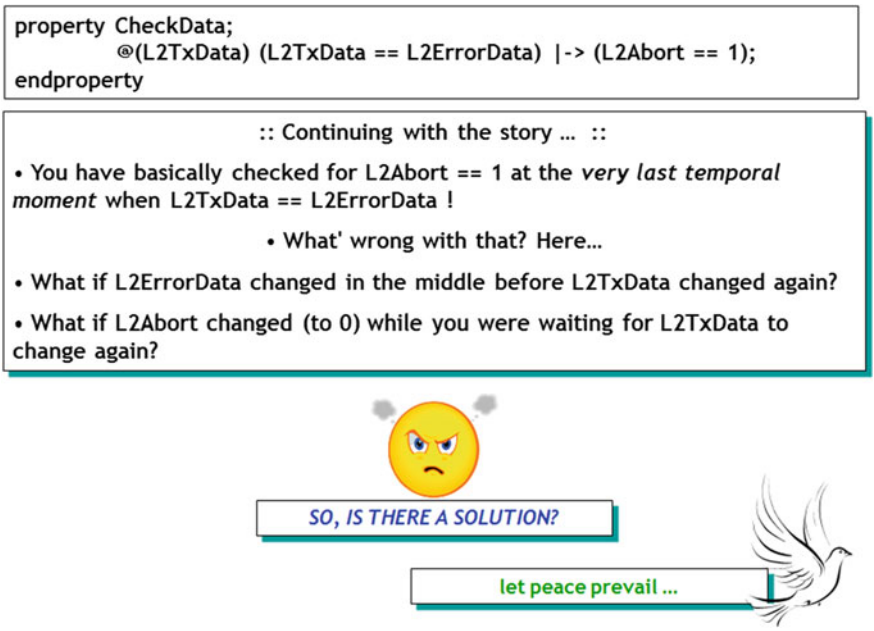


Fig. 15.2 Asynchronous assertion—problem statement analysis continued

We continue the analysis in Fig. 15.2. The annotation explains the reasons for frustration!!

In order to circumvent the problem we just described in Fig. 15.3, we can (unfortunately) continue with the asynchronous sampling edge, only that we put all the comparison expressions/variables as part of asynchronous sampling edge. This is shown in Solution 1 that will take care of the problems we first encountered. Think through and you will see why.

Why do we have assign #1 in solution 2? That way when L2TxData or L2Error DataW or L2ABortW change that there is a 1 time unit delay which will allow the new value to settle down –before- you check for (L2TxData == L2ErrorData).

This is a (convoluted) way to get around the check of these variables in the preponed region. If all this looks confusing, do not be daunted. I strongly advice you against using asynchronous edges as sampling edges. Again, if you are comfortable with using them, please do so, but be careful. Refer to the example above to help you with the behavior of asynchronous sampling edge. Note that I have shown all three solutions with asynchronous assertion (so much for my opposition to it!). How would you model this as a synchronous assertion? Please try and see if you succeed. Assume ‘posedge clk’ as your sampling edge.

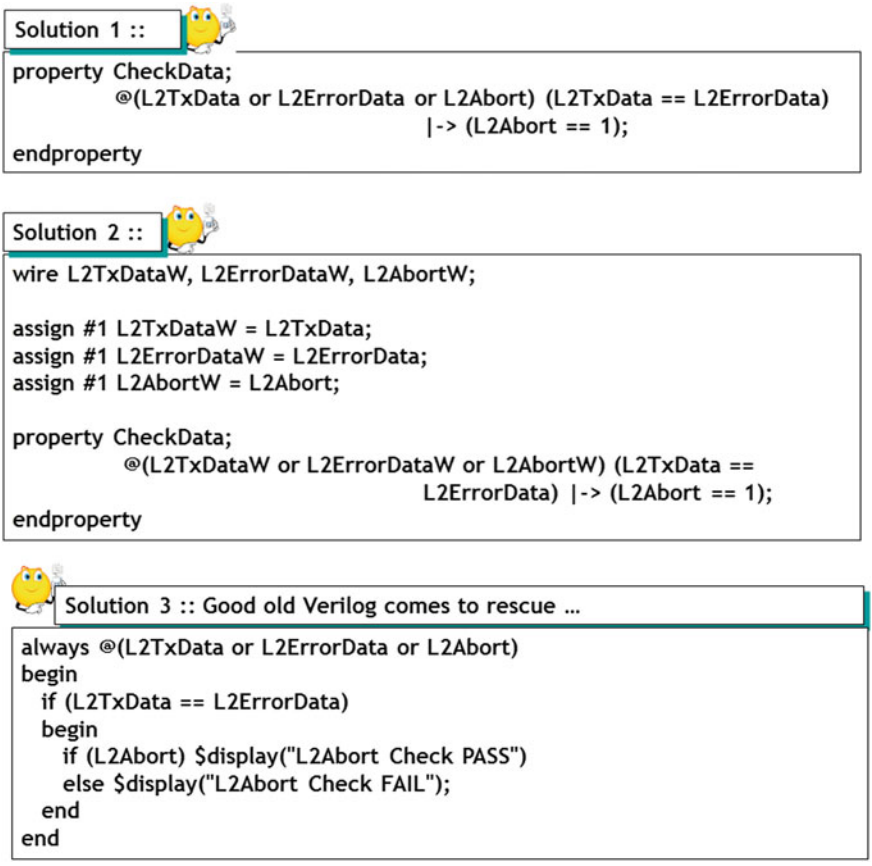


Fig. 15.3 Asynchronous assertion—solution

Solution 3 uses a procedural block to determine when you do the check. Notice that I have not used assertions in this solution. Point being, sometimes it is better and ok to simply use Verilog which will be more intuitive and give the results you desire. I recommend pure Verilog for asynchronous assertions and SVA for all other types of assertions.

Chapter 16
IEEE-1800-2009 Features

16.1 Strong and Weak Sequences

IEEE-1880-2009 adds the notion of a strong and weak operator applied to sequence expressions. The idea behind these 'strengths' is very simple.

Here's an example

```
property a_wait_b;
  @ (posedge clk) A |-> (A ##[1:$] B);
endproperty

  awb: assert property (strong(a_wait_b)) else $display($stime,"a_wait_b FAIL"); //default 'weak'
  awbc: cover property (weak(a_wait_b)) $display($stime,"a_wait_b PASS"); //default 'strong'
```

'strong' sequence means that if you run out of simulation ticks (mainly at the end of simulation, for example), the 'strong' sequence will FAIL. In other words 'strong' will evaluate to true only if there is a non-empty match of the sequence expression. And in yet other words, the 'strong' operator requires 'enough' ticks to witness a success. In our example, if 'B' never arrives until the end of simulation, the property will FAIL. By default, a sequence is 'weak' and as we have seen so far, if you run out of simulation ticks the sequence will not fail (a simulator may still give an indication of an incomplete sequence).

On the other hand, 'cover' is strong by default. Analogous to 'assert', if the property does not complete, the evaluation of sequence expression does not succeed and the 'cover' will be considered to FAIL (i.e. not covered). In other words, an incomplete 'cover' sequence will not give us a 'PASS' or 'cover' indication, because there haven't been enough ticks to reach a 'success' state. That is exactly what we want because we do not want an incorrect 'cover' of a sequence that never completes. On the other hand, if you use 'weak' operator with 'cover' and the sequence never completes, the 'cover' will be considered to have completed or

A. B. Mehta, *SystemVerilog Assertions and Functional Coverage*,
DOI: 10.1007/978-1-4614-7324-4_16,

covered (this is simulator dependent from author's experience, so take the description of cover with a 'weak' operator with a grain of salt).

In short, by default, a property is weak in the context of an 'assert' (or an 'assume') and is strong in the context of a 'cover'.

16.2 Deferred Assertions

Deferred assertions are a type of 'immediate' assertions. Recall that 'immediate' assertions evaluate immediately without waiting for variables in its combinatorial expression to settle down. This also means that the immediate assertions are very prone to glitches as the combinatorial expression settles down (for example, an expression evaluates to '0' then to '1' then back to '0' to settle down on '0'), the immediate assertion may fire multiple times. On the other hand, deferred assertions do not evaluate their sequence expression until the end of time tick when all values have settled down (or in the reactive region of the time tick).

The syntax for deferred immediate assertion is "assert #0". It's the #0 that distinguishes deferred immediate assertion from the immediate assertion.

Let us examine the following example (as it appears in the 2009 LRM).

```
assign not_a = !a;
always_comb begin:b1
  a1: assert (not_a !=a) //immediate
  a2: assert #0 (not_a !=a); //Deferred immediate
end
```

Let us examine the difference between immediate and deferred immediate assertions in this example. As soon as 'a' changes, always_comb wakes up and both the immediate and deferred assertions fire right away. Since this is an 'always_comb' block, it will actually trigger twice, one when 'a' changes and then when 'not_a' changes. When the immediate assertion fires, the continuous assignment "not_a = !a" may not have completed its assignment. In other words, 'a' has not been inverted yet. But the immediate assertion expects an inverted 'a' on 'not_a'. The assertion will fail. This is why immediate assertions are known to be glitch prone.

On the other hand, the deferred assertion will wait until all expressions in the given time stamp have settled down (in other words, it was put in the so-called deferred assertion report queue). In our case, the continuous assign would have completed its evaluation by the end of time stamp (meaning when the deferred assertion queue will be flushed); and 'not_a' would indeed be = !a. This is the value the deferred assertion will take into account when evaluating its expression. The deferred assertion will pass.

Another feature of deferred immediate assertion to note is that it can be declared both in the procedural block as well as outside of it (recall that immediate assertion can only be declared in procedural block). For example, following is legal for deferred immediate assertion but not for immediate assertion.

module (x,y,z);

…..

z1: **assert #0** (x == y ||z);

endmodule

This is actually equivalent to

module (x,y,z);

always_comb begin

z1: **assert #0** (x == y||z);

end

endmodule

16.3 $changed

SystemVerilog 2009 adds $changed sampled value function in addition to the ones we have already seen such as $past, $rose, $fell and $stable (Fig. 16.1).

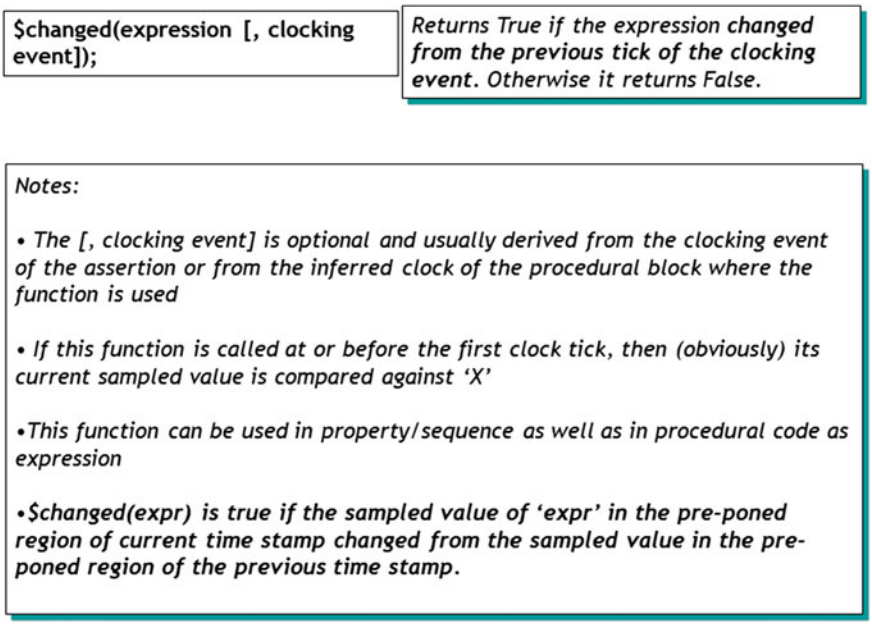
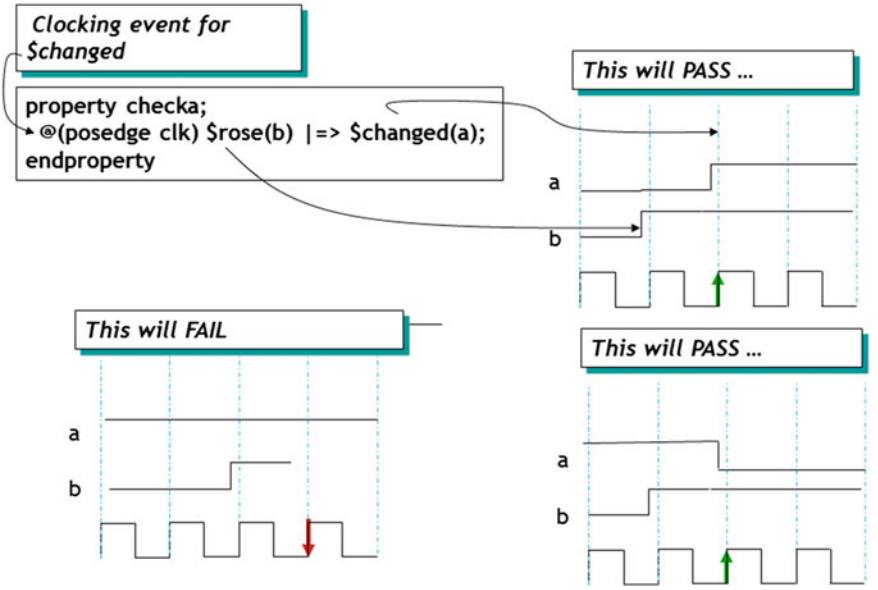


Fig. 16.1 $changed



16.4 $sampled

$sampled simply does—explicitly—what we have seen assertions do. In other words, the expressions in an assertion are always sampled in the preponed region of a time stamp. $sampled does exactly the same. It returns the value of the expression sampled in the preponed region of the simulation time stamp in which the function was called.

So, *for concurrent assertions $sampled function is redundant*. Following two are equivalent

```
z1: assert property (@ (posedge clk) $sampled(a) == $sampled(b));
z1: assert property (@ (posedge clk) a == b));
```

The reason they are the same is that in the concurrent assertion (as we have seen throughout the book) the expressions are always sampled in the preponed region of the time stamp in which they are sampled. $sampled function also returns value of expression in the preponed region.

However, there are places it can be useful for debug purpose. For example, in a simultaneously changing event situation, you can find out the sampled value (i.e., the value in the preponed region). Let us say, you have an assertion where you want to make sure that 'gnt' is asserted on a posedge clk. If 'gnt' and posedge clk went high at the same time, the property will fail. That's because the sampled value of 'gnt' is 0 in the preponed region. In such a case you can have a $display("gnt=%b", $sampled(gnt)); This will tell you right away that the sampled value was '0' which is why the assertion failed.

16.5 $past_gclk, $rose_gclk, $fell_gclk, $stable_gclk, $changed_gclk, $future_gclk, $rising_gclk, $falling_gclk, $steady_gclk, $changing_gclk

As the name suggests, these sampled value functions work off of a global clock. Before we look into these functions, let us see what a global clock is.

```
module top_pd;
  logic clk;
  global clocking sys_clk @ (clk); endclocking
  ….
endmodule
```

'sys_clk' is now considered a global clocking event. It is defined to occur (trigger) if there is a change in 'clk'. You can access global clock using the system function $global_clock. This system function does not take any arguments but returns the event expression specified in the global clocking declaration.

Let us revert to the system functions. *These functions can only be used if there is a global clock defined in your test-bench* (hence the _gclk suffix). They are sampled value functions as we have seen before and they sample their expression value at the global clock tick that you have defined. These sampled value functions are divided into two groups. One groups looks in the past (these are identical in functionality with the sampled value functions we have seen previously only that the _gclk sampled value functions work off a global clock event). The other group has 'future' sampled value functions. They sample the value of the expression in the time step that subsequently (and immediately) follows the time step in which the function is called. Note that the 'past' sampled value functions have a non-global clock counterpart as we have seen. *However, for the 'future' sampled value functions, there is no non-global clock counterpart*. They work only if you have defined a global clock.

The *past* sampled value functions are

$past_gclk (expression)

$rose_gclk (expression)

$fell_gclk (expression)

$stable_gclk(expression)

$changed_gclk(expression)

The *future sampled value functions* are

$future_gclk(expression)

$rising_gclk(expression)

$falling_gclk(expression)

$steady_gclk(expression)

$changing_gclk(expression)

As mentioned before the globally clocked *past* sampled value functions work the same way as the non-global clocking sampled value function.

If you recall, these past sampled value functions take an explicit clocking event. So, $rose_gclk (expr) is equivalent to $rose(expr, @ $global_clock). Please refer to the non-global clocking past sampled value functions to understand how these functions work (Chap. 5)

The future sampled value functions are also similar except that they use the subsequent (future) value of the expression. Here's a brief explanation of each.

$future_gclk(expression) returns the sampled value of expression at the next global clocking tick

$rising_gclk(expression) returns a Boolean True if the sampled value of the *least significant bit* of the expression changes to 1 at the next global clocking event. Else it returns false.

$falling_gclk(expression) returns a Boolean True if the sampled value of the *least significant bit* of the expression changes to 0 at the next global clocking event. Else it returns false.

$steady_gclk(expression) returns a Boolean True if the sampled value of the expression does not change at the next global clocking event. Else it returns false

$changing_gclk(expression) returns a Boolean True if the sampled value of the expression changes at the next global clocking event. Else it returns false.

A few points on future samples value functions:

1. *The 'future' sampled value functions cannot be used outside of concurrent assertions.*
2. They cannot be nested (for example, $future_gclk ($falling_gclk(gnt_) && req)). But do not confuse this with the following which is legal
   F1: assert property (@ global _clock $rising_gclk(sig1) |-> $falling_gclk(sig2));
3. They cannot be used in a 'reset' condition (for example, "disable_iff ($falling_edge (reset_)").

Note also that neither the past nor the future sampling functions can be used in an assertion *action block (pass or fail).*

As of this writing, none of the popular simulators supported these functions. Hence, the author is not able to show their workings with a simulation log.

16.6 'triggered'

Recall the .ended method (Chap. 11) which attaches to a sequence .ended can be used anywhere in a sequence where you want to check for another sequence to have ended. The only difference between .ended and .matched is that .ended must have the same clock used in both the sequences in play while .matched can have different clocks.

The 2009 standard gets rid of .ended and in place supports .triggered. In other words, .triggered has the same exact meaning as .ended, only that .triggered can be used both where .ended gets used as well as where .triggered was allowed. In other words, .triggered can be used both in a sequence as well as in procedural block and also in level sensitive 'wait' statement.

Following from the 1800-2009 LRM:

IEEE Std 1800-2005 17.7.3 required using the .ended sequence method in sequence expressions and the .triggered sequence method in other contexts. Since these two constructs have the same meaning but mutually exclusive usage contexts, in this version of the standard, the .triggered method is allowed to be used in sequence expressions, and the usage of .ended is deprecated and does not appear in this version of the standard.

Please refer to the (Sect. 11.1) on .ended to understand .triggered in detail. I am leaving .ended in the book, for the sake of completeness and to be compatible with 1800-2005 standard.

Here's an example of .triggered usage in a procedural assignment using level sensitive control.

```
sequence busGnt;
  @ (posedge clk) req ##[1:5] gnt;
endsequence

initial begin
  wait (busGnt.triggered) $display($stime,,,"Bus Grant given");
end
```

Here's an example that is identical to the use of .ended in sequences.

```
sequence abc;
  @ (posedge gclk) a ##[1:5] ##1 b [*5] ##1 c;
endsequence

sequence myseq;
  @ (posedge gclk) d ##1 abc.triggered ##1 !d;
endsequence
```

16.7 'followed by' Property #-# and #=#

The *followed by* properties has the following form.

sequence_expression #-# property_expression

sequence_expression #=# property_expression

#-# is the overlapped property and # = # is the non-overlapped, just as in |-> and |=> but there are differences between the implication operators and the *followed by* operators.

For *followed by* to succeed both the antecedent sequence_expression and the consequent property_expression must be true. *If the antecedent sequence_expression does not have any match then the property fails*. If the sequence_expression has a match then the consequent property_expression must match. This is the fundamental difference between the implication operators (|-> and |=>) and the followed by operators. Recall that with implication operators, if the antecedent does not match, you get a vacuous pass and not a fail.

Obviously, #-# being an overlapped operator, it starts the consequent evaluation the same time that the antecedent match ends (and succeeds). Consequently, the #=# non-overlapped operator will start the consequent evaluation the clock after the antecedent match ends and succeeds.

Here's simple example

```
property p(a, b)
  @ (posedge clk) a #=# b;
endproperty

assert property (p(req[*5],gnt));
```

Request need to remain asserted (high) for five consecutive clocks. One clock later gnt must be asserted (high). If request does *not* remain asserted for five consecutive clocks, the assertion will fail. If it does remain asserted for 5 clocks and the next clock gnt is not asserted, the assertion will fail. If both the antecedent and consequent match in the required temporal domain, the property will pass.

16.8 'always' and 's_always' Property

'always' property behaves exactly as you would expect. The syntax for 'always' (and it's variations) is

1. **always property_expression** (weak form)
2. **always [cycle delay constant range expression] property_expression** (weak form with unbounded range)

3. **s_always [constant_range] property_expression** (strong form with bounded range)

First, let us see how 'always' works. As LRM puts it "A property 'always property_expression' evaluates to true if and only if the property_expression holds at every current and future clock tick". Rather self-explaining. Here's a simple example.

property reset_always;

@ (posedge clk) POR[*5:10] |=> **always** !reset;

endproperty

The property says that once POR (power on reset) signal has remained high for minimum 5 clocks or maximum 10, that starting next clock, reset would remain de-asserted 'always' (forever).

'always' makes it simple to specify the continuous longevity of an assertion.

Next, let us see how always [cycle delay constant range] works.

property p1;

@ (posedge clk) a |-> **always** [3:$] b;

endproperty

property p1 says that if 'a' is true that 'b' will be true 3 clocks *after* 'a' and will remain true 'always' (forever) after the 3 clocks. Note that 'always[n:m]' allows an unbounded range.

In contrast 's_always' allows only bounded range.

So, let us see what s_always does

property p2;

@ (posedge clk) a |-> **s_always** [3:10] b;

endproperty

The property says that if 'a' is true that 'b' remains true from 3rd clock to 10th clock after 'a' was detected true. This is a 'strong' property (hence the suffix 's_'). Recall strong property that we discussed earlier. This 's_' property also works the same way. In other words, if you run out of simulation ticks for 's_always', the property will indeed fail.

BUT, why do we need 'always'? Don't the concurrent assertions always execute at every clock tick? The answer is yes which means we do not always need an 'always' operator with a concurrent assertion. It is redundant. For example, in the following 'always' is redundant.

P1: **assert property** p1p (@ (posedge clk) **always** bstrap1==0);

There is no reason for an 'always' in the above concurrent assertion. It is the same as

P1: **assert property** p1p (@ (posedge clk) bstrap1==0);

'always' can be useful in 'initial' block, however. See the example below

initial begin P1: **assert** p1p (@ (posedge clk) always bstrap1==0);

Note that the immediate property noted above is slated to execute only once. In our case though once it is asserted, it will then look for bstrap1==0 at every posedge clock.

Bottom line: 'always' is not very useful for concurrent assertions outside of procedural blocks. In immediate or concurrent assertions within a procedural block there is limited use. Again, none of the simulators that author tried had this feature implemented. Hence, my apology in advance if I've missed some critical point here. LRM does not make it any further clear either.

16.9 'eventually', 's_eventually'

Well, we all want something to happen 'eventually' in an assertion (hopefully)! There are two types of this operator, the 'weak' kind ('eventually') and the 'strong' kind ('s_eventually'). Here are three forms of these two properties.

s_eventually property_expr (strong property without range)

s_eventually [cycle_delay_constant_range] property_expr (strong property with range)

- the constant_range can be unbounded

eventually [constant_range] property_expr (weak property with range)

- the constant_range must be bounded

Some examples

property p1;

s_**eventually** $fell(frame_);

endproperty

Eventually PCI cycle will start with assertion of frame_. If frame_ does not assert (low) until the end of simulation time, the property will fail since this is a strong property. Note that frame_ can be true in current clock tick or any future clock tick.

property p2;

s_eventually [2:5] $fell(frame_);

endproperty p2;

A new PCI cycle must start (frame_ to go low) within the range of 2 clocks from now (i.e. frame_ cannot assert earlier than the 2nd clock) and eventually by 5th clock (2nd and 5th clock inclusive).

Exercise: Is the property 'p3' equivalent to 'p2' above? Hint: Simulate from 'initial' condition to know the subtle difference.

property p3;

frame_ |-> ##[2:5] $fell(frame_);

endproperty

Following is s_eventually with unbounded range.

property p4;

s_eventually [2:$] $fell(frame_);

endproperty

A new PCI cycle must start (from the current clock tick) 2 clocks from now (i.e. frame_ cannot assert earlier than the 2nd clock) or any time after that.

property p4;

eventually [2:$] $fell(frame_); //*ILLEGAL*. Weak property must be bound.

endproperty

property p4; //Courtesy LRM 1800-2009

s_eventually always a;

endproperty

'a' (boolean) will eventually (starting current clock tick) go high and then remain high at every clock tick after that until the end of simulation.

16.10 until, s_until, until_with and s_until_with Properties

There are 4 forms of 'until' property

1. property_expression1 **until** property_expression2 (weak form—non-overlapping)
2. property_expression1 **s_until** property_expression2 (strong form—non-overlapping)

3. property_expression1 **until_with** property_expression2 (weak form—overlapping)
4. property_expression1 **s_until_with** property_expression2 (strong form—overlapping)

Let us start with 'until'.

```
property p1;
  req until gnt;
endproperty
```

property p1 is true if 'req' is true until 'gnt' is true. In other words, 'req' must remain true as long as 'gnt' is false. 'req' need not be true at the clock tick when 'gnt' is found to be true. If 'gnt' is never true, 'req' will remain true at every current and future clock tick. Since 'until' is of weak form, if this property never completes (i.e. 'gnt' is never true), the property will *not* fail.

```
property p1;
  req s_until gnt;
endproperty
```

s_until is identical to 'until' except that if 'gnt' never arrives and you run out of simulation time, the property will fail.

until_with is also similar to 'until'.

```
property p1;
  req until_with gnt;
endproperty
```

property p1 is true if 'req' is true until (and *including*) a clock tick when 'gnt' is true. In other words, 'req' must remain true as long as 'gnt' is false. 'req' must be true at the clock tick when 'gnt' is found to be true. If 'gnt' is never true, 'req' will remain true at every current and future clock tick. Since 'until_with' is of weak form, if this property never completes (i.e. 'gnt' is never true), the property will *not* fail.

In short, property 'until_with' requires 'req' and 'gnt' to be true at the same clock tick when 'gnt' is found to be true. 'until' does not have this requirement.

```
property p1;
  req s_until_with gnt;
endproperty
```

Same as 'until_with' but if you run out of simulation tick (end of simulation, for example), and if 'gnt' is never found to be true, this property will fail.

16.11 nexttime and s_nexttime

'nexttime' property_expression evaluates to true, if property_expression is true at time t+1 clock tick.

There are 4 forms of 'nexttime'.

nexttime property_expression (weak form)

The weak nexttime property **nexttime** *property_expr* evaluates to true if, and only if, either the

property_expr evaluates to true beginning at the next clock tick or there is no further clock tick.

s_nexttime property_expression (strong form)

The strong nexttime property **s_nexttime** *property_expr* evaluates to true if, and only if, there

exists a next clock tick and *property_expr* evaluates to true beginning at that clock tick.

nexttime [constant_expression] property_expression (weak form)

The indexed weak nexttime property **nexttime** [*constant_expression*] *property_expr* evaluates to

true if, and only if, either there are not *constant_expression* clock ticks or *property_expr* evaluates to

true beginning at the last of the next *constant_expression* clock ticks.

s_nexttime [constant_expression] property_expression (strong form)

The indexed strong nexttime property **s_nexttime** [*constant_expression*] *property_expr*

evaluates to true if, and only if, there exist *constant_expression* clock ticks and *property_expr*

evaluates to true beginning at the last of the next *constant_expression* clock ticks.

Let us examine the following simple example.

```
property p1;
  @ (posedge clk) nexttime req;
endproperty
```

The above property says that the property will pass, if the clock ticks once more and 'req' is true at the next clock tick (t+1). In addition, since this is the weak form, if you run out of simulation ticks (i.e. there is no t+1), this property will *not* fail.

Following from LRM.

What if you want to check to see that 'req' remains asserted for all the clocks following the next clock? Following will do the trick.

property p1;

@ (posedge clk) **nexttime always** req;

endproperty

Or what if you want to see that starting next clock, 'req' will eventually become true? Following will do the trick.

property p1;

@ (posedge clk) **nexttime eventually** req;

endproperty

What if you want to see that 'req' is true after a certain exact # of clocks. Following will do the trick

property p1;

@ (posedge clk) **nexttime[5]** req;

endproperty

This property says that 'req' shall be true at the fifth future clock tick (provided that there are indeed 5 clock ticks in future, of course).

property p1;

@ (posedge clk) **s_nexttime** req;

endproperty

Same as 'nexttime' except that if you run out of simulation ticks after the property is triggered (i.e. there is no (t+1), the property will fail. Other way to look at this is that there exists a next clock and 'req' should be true at that next clock, else the property will fail.

Similarly, the following property says that there must be at least 5 clock ticks and that 'req' will be true at the fifth future clock tick.

property p1;

@ (posedge clk) **s_nexttime**[5] req;

endproperty

Having said all this, what is the difference between 'nexttime' and ## delay? Why aren't the following two equivalent?

@ (posedge clk) nexttime[5] req;

@ (posedge clk) ##5 req;

Well the above two are indeed equivalent. So, why do we need 'nexttime'? Since none of the simulators at the time of writing this book supported this feature,

the author was not able to simulate different scenarios to find a true advantage. The author believes that 'nexttime' is easier to use in complex sequences and more readable. Also, it allows the strong ('s_') and weak properties that determine the behavior of the simulation outcome if there is no time tick 't+1'. This is not possible with '##' operator. Here's an example of use of 'nexttime' in a semi-complex sequence.

Property

@ (posedge clk) (seq1.**matched nexttime** seq_expr == 'hff);

endproperty

When 'seq1' ends(matches) at 't' that the next time tick ('t+1') 'seq_expr' must be equal to 'hff.

16.12 Case Statement

The *case* statement in assertions is the same as the one we use in systemverilog language. There is no difference, only that in systemverilog assertions, you use the *case* statement in a property. The *case* property statement is a multi-way decision making mechanism that tests a boolean expression and sees if it matches one of a number of boolean expressions. On a match, it will take action specified for that case statement. We are all familiar with this functionality of *case*. The 'default' statement is optional.

Here is a simple example.

property CycleCase (logic [1:0] CycleType);

case (CycleType)

2'b00: $fell(frame_) ##1(cmd==READ);
2'b01: $fell(frame_) ##1(cmd==WRITE);
2'b10: $fell(frame_) ##1(cmd==TABORT);
2'b11: $fell(frame_) ##1(cmd==MABORT);

default: $fell(frame_) ##1 (cmd==ILLEGAL); //default is optional

endcase

endproperty

Note that if the default statement is not given and all of the comparisons fail, then none of the case item property statements are evaluated. In addition, as we know if "assert property ()" antecedent does not evaluate to true that we get a vacuous pass. The same applies here. *If there is no default and no case branch match, we get a vacuous pass.* Do make a note of this.

16.13 $inferred_clock and $inferred_disable

Many times while developing assertion logic, we define default blocks for clock and reset. These default blocks based clock and reset are then available in properties that follow. Please refer to the (Sect. 4.3.1) on Default Clocking for further understanding of a default-clocking block.

Let us say you have the following default blocks:

module (…,clk, rst,…);

default clocking negclock @ (negedge clk); **endclocking**

default disable iff rst;

One of the ways to use this default clocking and reset blocks is as follows.

property inferB(a, b, c, clk=$inferred_clock, reset=$inferred_disable);

@ (clk) disable iff (reset) a |=> b || c;

endproperty

assert property (inferB(x, y, z));

The formal parameters of property inferB uses default clocking and reset from their respective default blocks. In other words, @ (clk) is now @ (negedge clk).

Note that if property 'inferB' is invoked as follows, the $inferred_clock will not take effect—but the actual clocking event 'posedge clk' will take effect

assert property inferB (a, b, c, posedge clk, reset);

@ (clk) in property inferB will be '@ (posedge clk)' and not '@ (negedge clk)' as in the default clocking block. In other words, the actual overwrites the formal argument, as always.

From the above we can see that the inferred clocking event expression is the current resolved event expression that can be used in a clocking event. Of course, if you use $inferred_clock and there is no default clocking block defined, you will get an Error.

16.14 Let Declarations

We have all used the compiler directive 'define (which is a global text substitution macro). Note the word global—it is truly global spanning across all scopes of your design modules and files. For example, 'define intr 3′b111 will substitute 'intr with 3′b111 where ever it sees 'intr either within the local scope or global scope. This

can be good and bad. Good is that you have to define it only once and it will span across module/file boundaries. Bad is you cannot redefine ‘intr (well actually you indeed can, but with consequences). For example, if you change the definition of ‘intr in a package, you will get a warning and also the new definition will overwrite all the previous ones. Also, ‘define is not parameterizable.

That is where ‘let’ comes into picture. ‘let’ not only allows local scope but also allows parameterization (as in a sequence or a property). Parameterization is a big advantage as you can imagine towards developing modular and reusable code.

The syntax for ‘let’ is

let_declaration::= let let_identifier [([let_port_list]) = expression;

Let us see each feature of ‘let’ one by one.

16.14.1 Let: Local Scope

Let us examine the following example. First let us see an example using ‘let’

```
module example;

logic r1,r2, r3,r4,clk,clk1;

let exDefLet = r1 || r2;

always @ (posedge clk) begin :ablock

  let exDefLet = r1 & r2; //exDefLet has a local scope of ‘ablock’

  r3=exDefLet;

end

always @ (posedge clk1) begin : bblock

  r4=exDefLet; //exDefLet will take the definition from the scope that is visible to
  it. Here

//it is the outer most scope definition of (r1 || r2);

end

endmodule
```

We have defined two definitions of ‘exDefLet’. One in the always block ‘ablock’ and another in ‘bblock’. Note that their definition (expression) is different in each block. Since ‘let’ can have local scope, each of the definition of ‘let’ will be preserved in its local block. The above code will look like the following after ‘let’ substitutions take place

```
module example;

logic r1,r2, r3,r4,clk,clk1;

always @ (posedge clk) begin :ablock
  r3=r1 & r2;
end

always @ (posedge clk1) begin : bblock
  r4=r1 || r2;
end

endmodule
```

If the same design was modeled using ‘define here’s how the code would look like

```
module example;

logic r1,r2, r3,r4,clk,clk1;

‘define exDefLet r1 || r2;

always @ (posedge clk) begin :ablock
  ‘define exDefLet r1 & r2;
  r3=exDefLet;
end

always @ (posedge clk1) begin : bblock
  r4=exDefLet;
end

endmodule
```

In this example, since there are two ‘define for the same variable, the compiler will complain right off the bat and use the second definition r1&r2 (it’s the latest in lexical order) as the global definition of exDefLet. The above code will look like the following after ‘define substitutions

```
module example;

logic r1,r2, r3,r4,clk,clk1;
```

```
always @ (posedge clk) begin :ablock
  r3=r1 & r2;
end

always @ (posedge clk1) begin : bblock
  r4=r1 & r2;
end

endmodule
```

As you see 'let' is very useful from scoping point of view. It follows the normal scoping rules. You can parameterize it and reuse the 'let' expression repeatedly with different parameters. Let us now see some more usage/advantages of 'let'.

16.14.2 Let: with Parameters

As mentioned before, 'let' can be parameterized which is its significant advantage over 'define which is purely a text substitution macro (global compiler directive). Note that instantiation of 'let' is quite different from a 'parameterized function'. With 'let' you replace the instance with entire 'let' body. With 'function' you simply pass the parameters and the function executes using those parameters. Function does not replace the instance of function call.

Ok, let us see a simple example.

```
module abc;

logic clk, x, y, j;

logic [7:0] r1;

let lxor (p, q=0) = p^q;

always @ (posedge clk) begin
  for (i = 0; i <= 256; i++) begin
      r1 = lxor(i);
  end
end
```

endmodule

For each value of 'i' r1 will get the 'xor' of 'I' and 'q=0'. Note that the formal parameter 'q' is assigned a default actual value of '0'. That being the case, when "r1=lxor(i)" is executed, the actual 'i' replaces p in lxor and 'q' takes on its assigned default value of '0'. You could have also specified "r1=lxor(i,j)" and the formal 'q' will now take the value of 'j' (whatever 'j' is).

Note that some rules apply to the formal arguments.

1. Note again that the 'let' body gets expanded with the actual arguments (which replace the formal arguments) and the body (RHS of 'let') will replace the instance of 'let'. That being the case, once the body of 'let' replaces the instance of 'let', all required semantic checks will take place to see that the expanded 'let' body with the actual arguments is legal.
2. The formal arguments can have a default value (as we have seen in the example above).
3. The formal arguments can be typed of un-typed. The typed arguments will force type compatibility between formal and actual (cast compatibility). In other words, the actual argument will be cast to the type of the formal argument before being substituted. Un-typed formal in that case is more flexible.
4. If the formal argument is of 'event' type, then the actual argument must be an event_expression.
5. If the variables used in 'let' are not formal arguments to the 'let' declaration, they will be resolved according to the scoping rules of the scope in which 'let' is declared.

16.14.3 Let: In Immediate and Concurrent Assertions

Yes, 'let' can be used in an immediate ('assert') as well as concurrent ('assert property') assertions in a procedural block.

Let us start with a very simple example of 'let' usage in a sequence. *Note that 'let' expression can only be structural or with sampled value function (as in $past).* We will see 'let' with sampled value function in the next section.

```
module abc;

logic req, gnt;

let reqack = !req && gnt;

sequence reqGnt;

  reqack;

endsequence
```

endmodule
After expanding the 'let' instance

module abc;

logic req, gnt;

sequence reqGnt;

!req && gnt; //

endsequence

endmodule

Here's another example.

module abc;

logic clk, r1,r2,req,gnt;

let xxory (x,y) = x ^ y; //bit wise xor

let xory = req || gnt;

….

P1: **assert property** (@ (posedge clk) (xory)); //concurrent assertion

always_comb begin

a1: **assert** (xxory (r1,r2)); //immediate assertion

a2: **assert** (xory);

end

endmodule

After expansion (showing complete hierarchical scope)

module abc;

logic clk, r1,r2,req,gnt;

```
P1: assert property (@ (posedge clk) (abc.req || abc.gnt)); //concurrent assertion

always_comb begin
a1: assert (abc.r1 ^ abc.r2)); //immediate assertion

a2: assert (abc.req || abc.gnt);

end

endmodule
```

Now, here's an example that uses the sampled value function $(rose) and $(fell).

```
module abc;

logic clk,r1,r2,req,gnt,ack,start;

let arose(x) = $rose(x);

let afell(y) = $fell (y);

always_comb begin

if (ack) s1: assert(arose(gnt));

if (start) s2: assert(afell(req));

end
```

Finally, here's where a 'let' can be declared

- module
- interface
- program
- checker
- clocking block

16.15 'restrict' for Formal Verification

The 'restrict' property is strictly for Formal (static functional) verification. *Simulators do not check this property*. Since we are not covering Formal Verification in this book, this property is noted here for the sake of completeness. As we saw with

the 'assume' property, formal verification requires some assumption or restriction in order for it to not explode in the state space. 'restrict' has the same semantics as 'assume', only that '*restrict' does not have an action block*. Here is the syntax.

restrict property (property_spec); //Note, no action block.

For example, for Formal Verification you need to restrict the checking of an assertion which has 5 inputs (a, b, c, d, e) and 2 control bits (x, y). If {x, y} = 2′b00, inputs a, b are of no use. We can restrict the static functional evaluation to not bother with a, b as follows

restrict property (@ (posedge clk) {x, y} == 2′b00);

Note again that the property is ignored by simulation. In other words, {x,y} == 2′b00 is not enforced during simulation.

Please refer to the (Chap. 13) on 'assume' to understand usage of 'restrict'.

16.16 Abort Properties: reject_on, accept_on, sync_reject_on, sync_accept_on

Recall 'disable_iff' disable condition, which preempts the entire assertion, if true. 'disable_iff' is an asynchronous abort (or reset) condition for the entire assertion. It is also asynchronous in that it's expression is not sampled but the expression is evaluated at every time stamp (i.e. in-between clock ticks as well as at the clock ticks) and whenever the 'disable_iff' expression turns true that the assertion will be abandoned (no pass or fail).

With that background, 1800-2009 adds four more abort conditions. 'reject_on' and 'accept_on' are asynchronous abort conditions (as in disable_iff) and 'sync_reject_on' and 'sync_accept_on' are synchronous (i.e. sampled) abort condition. Note that 'accept_on' is an abort condition for PASS, even though that may seem a bit counterintuitive at first. In other words, if 'accept_on' aborts an evaluation, the result is a PASS. If 'reject_on' aborts an evaluation, the result is FAIL.

The syntax for all four is the same.

accept_on (abort condition expression) property_expression

sync_accept_on (abort condition expression) property_expression

reject_on (abort condition expression) property_expression

sync_reject_on (abort condition expression) property_expression

Before we see examples, here are high-level points to note

1. One note off the bat to distinguish 'disable_iff' from the abort properties is that 'disable_iff' works at the concurrent assertion level while these abort properties

work at the property level. Only the property_expression associated with the abort property will get 'aborted'—not the entire assertion as with 'disable_iff'. More on this later.
2. The operators accept_on and reject_on operators work at the granularity of simulation time step (i.e. asynchronously).
3. In contrast, the operators sync_accept_on and sync_reject_on do *not* work at the granularity of simulation time-step. They are evaluated at the simulation time step of the clocking event.
4. You can nest the four abort operators accept_on, reject_on, sync_accept_on, sync_reject_on. Note that nested operators are in the lexical order accept_on, reject_on, sync_accept_on and sync_reject_on (from left to right).
5. Abort condition cannot contain any reference to local variables or the sequence methods .triggered and .matched.

Now let us look at some examples to nail down the concepts.

```
property p1;
  @ (posedge clk) $fell(bMode) |-> reject_on(bMode) data_transfer[*4];
endproperty

assert property (p1);
```

The above example specifies that on the falling edge of burst Mode (bMode), data_transfer should remain asserted for four consecutive clocks and that the bMode should –not- go high during those 4 data transfers. The way the property reads is; look for the falling edge of bMode and starting that clock reject (fail) the property (data_transfer[*4]) if at any time (i.e. asynchronously—even between clock ticks) it sees bMode going high. As noted before, 'reject_on' abort means failure. Hence consequent will FAIL and so will the property p1.

The important thing to note here is that the evaluation of the abort property namely "data_transfer[*4]" and the reject condition reject_on(bMode) start at the same time. In other words, (as shown below), this is like a 'throughout' operator where the LHS is checked to see if it holds for the entire duration of RHS. Similarly, here we check to see that while we are monitoring "data_transfer[*4]" to hold that bMode should not go high. If it does go high at any time during "data_transfer[*4]" the property will be rejected i.e. it will fail.

The same property can be written using sync_reject_on, only that the "bMode" will not be evaluated asynchronously (any time including in-between clock ticks) but will be sampled only at the sampling edge, clock tick.

Note that the above property can be written using 'throughout' as well. Please refer to (Sect. 6.9) on 'throughout' operator to see a similar example.

```
property p1;
  @ (posedge clk) $fell(bMode) |-> !(bMode) throughout data_transfer[*4];
endproperty
```

assert property (p1);

Let us look at an example of 'accept_on'

property reqack;

@ (posedge clk) **accept_on**(cycle_end) req |-> ##5 ack;

endproperty

assert property (reqack);

This property uses "accept_on(cycle_end)" as the abort condition on the property "req |-> ##5 ack". When 'req' is sampled high on a posedge clk, the property "req |-> ##5 ack" starts evaluating waiting for ack to arrive after 5 clocks. At the same time, 'cycle_end' is also monitored to see if it goes high. Here are the scenarios that take place.

'cycle_end' arrives within the 5 clocks that the property is waiting for 'ack'. The accept_on condition will be true in that case and the property will be considered to pass. The next evaluation will again start the next time 'req' is sampled high on posedge clk.

'cycle_end' does not arrive within 5 clocks when the property is waiting for 'ack'. The property will evaluate as with any concurrent assertion and if 'ack' does not come in high after 5 clocks, the property will fail.

'cycle_end' arrives exactly the same time as 'ack' within the 5 clocks. The abort condition takes precedence. Since in this case, both 'ack' arrived and the accept_on was triggered at the same time, the accept_on aborts the evaluation with a pass and so the assertion will pass. What if we used 'reject_on' instead of 'accept_on' in such a scenario?

In short, the property evaluation aborts on 'accept_on' (and passes) or 'reject_on' (and fails) OR it will finish on its own (and pass/fail) if the abort condition does not arrive.

Here are some more examples courtesy 1800-2009 LRM.

property p; (**accept_on**(a) p1) and (**reject_on**(b) p2); **endproperty**

Note that we are using an 'and' operator here between two properties p1 and p2. Note that for an 'and' to succeed both the LHS and RHS of 'and' must complete and pass. If 'a' becomes true then p1 will abort and pass. But since there is an 'and' we will wait for the second property to complete as well. If 'b' becomes true during the evaluation of p2, p2 will be considered to fail and since this is an 'and' the property 'p' will fail. What if we used an 'or' instead?

property p; (**accept_on**(a) p1) or (**reject_on**(b) p2); **endproperty**

Recall that 'or' requires either the LHS or the RHS to complete and pass. In the same scenario as above, if 'a' becomes true first during the evaluation of p1, p1 is aborted and will be pass (i.e. accepted) and the property 'p' will pass.

Note that nested operators are in the lexical order accept_on, reject_on, sync_accept_on and sync_reject_on (from left to right). If two nested operator conditions become true in the same time tick during the evaluation of the property, then the outermost operator takes precedence.

property p; **accept_on**(a) **reject_on**(b) p1; **endproperty**

Note there is no operator between accept_on and reject_on.

If 'a' goes high first, the property is aborted on accept_on and will pass. If 'b' goes high first, the reject_on succeeds and the property p will fail. If both 'a' and 'b' go high at the same time during the evaluation of p1, then accept_on takes precedence and 'p' will pass.

One final note (and at the risk of sounding like a broken record), many of the 1800-2009 features were not supported by EDA vendor simulators at the time of writing this book. This is true for abort properties as well. Please try out these examples to see that the examples do adhere to the LRM and simulate correct. Author will greatly appreciate any incorrectness in the book.

16.17 $assertpassoff, $assertpasson, $assertfailoff, $assertfailon, $assertnonvacuouson, $assertvacuousoff

These system tasks add further control over assertion execution (or not) during simulation. We have seen $asserton, $assertoff and $assertkill (refer to Sect. 7.4) before. Here's a brief explanation of what these new system tasks do.

$assertpassoff: This system task turns off the action block associated with PASS of an assertion. This includes PASS indication because of both the vacuous and non-vacuous success (refer to Sect. 14.15). To re-enable the PASS action block, use **$assertpasson**. It will turn on the PASS action of both the vacuous and non-vacuous successes. If you want to turn on only the non-vacuous PASS then use **$assertnonvacuouson** system task. Note that these system tasks do not affect an assertion that is already executing.

$assertfailoff: This system task turns off the action block associated with the FAIL of an assertion. In order to turn it on, use **$assertfailon**. Here also, these system tasks do not affect an assertion that is already executing.

$assertvacuousoff system task turns off the PASS indication based on a vacuous success. An assertion that is already executing is not affected. By default, we get a PASS indication on vacuous pass.

All the system tasks take arguments, as we have seen before with $asserton, $assertoff and $assertkill (refer to Sect. 7.4). The first argument indicates how many level of hierarchy below each specified module instance to apply the system tasks. The subsequent arguments specify which scopes of the model to act upon (entire modules or instances).

16.18 Checkers

Checkers provide a way to group several assertions together into bigger block which acts with its well defined functionality and interfaces providing modularity and reusability. But wait. Don't we have 'modules' and 'interfaces' that do that same thing? You can indeed have a 'module' or 'interface' which can keep assertions separate from RTL code and bind them 'externally'.

Well, there are significant advantages to keeping assertions grouped into a checker.

1. A checker can be instantiated from a procedural block as well as from outside procedural code as with concurrent assertions. On the other hand, and as we are familiar with, a module cannot be instantiated in a procedural block. It can only be instantiated outside of a procedural block.
2. The formal parameters of a checker can be sequences, properties or other edge sensitive events. Module I/O ports do not allow this.
3. Synthesis tools normally ignore the entire checker block while in a module you have to use conditional compile if you have procedural code mixed with assertions.

Here's the syntax for a checker from LRM 1800-2009

checker checker_identifier [([checker_port_list])];

{checker_or_generate_item}

endchecker [: checker_identifier]

Let us start with a simple example.

1. module: First we'll define a '*module*' which holds properties and sequences for a simple bus protocol.
2. module test-bench: Then we'll define a test-bench module that instantiates this *module*.
3. Checker: Then we'll see how to put all these properties in a '*checker*checke' (instead of a module)
4. Checker Test-bench: And finally we'll see how the test-bench module 'calls' this *checker* from procedural code.

ONE: Assertions in a 'module'

```
module checkerM #(burstSize=4) (dack_, oe_, bMode, bMode_in, clk, rst);
input dack_, oe_, bMode, bMode_in, clk, rst;

  sequence data_transfer;

      ##2 ((dack_==0) && (oe_==0)) [*burstSize];

  endsequence

  sequence checkbMode;
```

```
    (!bMode) throughout data_transfer;
  endsequence

  property pbrule1;
    @ (posedge clk) disable iff (rst) bMode_in |-> checkbMode;
  endproperty

  checkBurst: assert property(pbrule1) else $display($stime,,,"Burst Rule Violated");
endmodule
```

module checkerM is a simple bus protocol checker that is fashioned on the PCI bus. When bMode(burst mode) is asserted (active low) for 2 clocks consecutively that we need to make sure that it remains low throughout data_transfer which is 4 clocks long. We have seen a very similar model in (Sect. 6.9) while studying *throughout*. Please refer to the AC specs (timing diagrams) for this checker module in that section. Note that we have parameterized the 'burstSize' which is a practical way to model a property that can be reused for different burst lengths.

Now let us see how do we instantiate this checkerM module from our test-bench.

TWO:

```
module test_checkerM (dataAck_, outputEn_, burstMode);
  output dataAck_, outputEn_, burstMode;
  logic bMode, bMode_send, rst, clk;
  ……..
  always @ (posedge clk or negedge rst) begin
     if (!rst) begin
          dataAck_=1'b0; outputEn_=0;burstMode=0;
  end
  /*Following block generates a bMode that is Low for 2 clocks consecutively. If so, we send it to the checkerM module. */
  always @ (posedge clk && rst) begin
```

```
    if (!bMode) begin

       @ (posedge clk);

      If (!bMode) bMode_send=bMode;

    end

  end

  //Now let us instantiate module 'checker_module'

  checkerM (#8)
   ck1(.dack_(dataAck_),.oe_(outputEn_),.bMode(bMode),.bMode_in(bMode
  _send),

  .clk(clk),.rst(rst));
endmodule
```

A few things to note here.

1. We had to explicitly create a 'sequence' in behavioral code since we cannot pass sequences to a module
2. We have to explicitly pass clk and rst to the module checkerM since a module instance won't inherit clk or rst from its context. In other words, clk and rst cannot be inferred from the module test_checkerM.
3. You cannot pass an edge control to a module (we all know how modules/instances work… so some of these points are probably obvious). But since an edge cannot be passed to a port, you have to make sure that you send the right polarity on these ports (clk for posedge clk) and (!clk for negedge clk)

Now let us model the same checkerM 'module' as a 'checker'

THREE:

```
checker checkerM #(burstSize =4) (dack_, oe_, bMode, bMode_in, rst);
                    Input dack_, oe_, bMode,clk, rst;

                    event clk = $inferred_clock;

                    default clocking @ clk; endclocking

                    sequence data_transfer;

                    ##2 ((dack_==0) && (oe_==0)) [*burstSize];

                    endsequence
```

```
        sequence checkbMode;
            (!bMode) throughout data_transfer;
        endsequence
        property pbrule1;
            @ (posedge clk) disable iff (rst) bMode_in |-> checkbMode;
        endproperty
        checkBurst: assert property (pbrule1) else $display($stime,,,
        "Burst Rule Violated");
endchecker
```

Note that 'clk' is now inferred from the context from which checkerM is called (see the next module test_checkerM). Also, we have defined a sequence bModeSeq that will be explicitly passed from the test_checkerM module. Neither of these two features are possible if we have modeled our assertions in a Verilog module.

Here's the test_checkerM module that calls the 'checker checkerM' module

FOUR

```
module test_checkerM (dataAck_, outputEn_, burstMode);

output dataAck_, outputEn_, burstMode;

logic cycle_start, rst, clk;
……..

/*Following block generates a bMode that is Low for 2 consecutive clocks. */

sequence bMode_Sequence;
  !burstMode[*2]
endsequence

……

//Now let us call module 'checker_module' from a procedural block

always @ (posedge clk or negedge rst) begin
  if (!rst) begin
   dataAck_=1'b0; outputEn_=0;burstMode=0;
```

end

else

checkerM (#8) ck1(.dack_(dataAck_),.oe_(outputEn_),.bMode(bMode),.bMode Seq(bMode_Sequence).rst(rst));

endmodule

Note

1. We did not explicitly pass 'clk' to the module checkerM. The clk was inferred from the context of the procedural block from which it was called (just as in concurrent assertion that is called from a procedural block). We could have done the same for 'rst'.
2. We passed a sequence bMode_Sequence to checkerM (as opposed to a signal to the module test_checkerM.

Now let us study further language features and nuances of a 'checker'.

Once again, the clock and reset (disable iff) contexts are inherited from the scope of the checker instantiation. Here is another simple example.

module test;

default clocking @ clk; endclocking

default disable iff reset;

checker test_bMode;

//directly inherits @ clk and 'reset' from the higher level context of //module test

endchecker

checker test_cMode;//Note this is a new checker

//Redefines the default blocks. Point is that you can infer/inherit or redefine //what is

//inherited

default clocking @ clk1; endclocking //Note that the default clocking block is //for @ clk1

default disable iff reset_system; //The default disable iff condition is for //reset_system

endchecker

endmodule

The example shows a test-bench called 'module test' which defines a clk and a reset at 'module test' level. The first checker 'test_bMode' inherits the clk and reset from its higher-level scope (which is 'module test'). The second checker 'test_cMode' defines its own clk1 and reset_system. This enables it to have its own local definition of clk1 and reset_system. It will not inherit the default clk and reset from the top level module 'module test'.

16.18.1 Nested Checkers

As mentioned earlier, a checker can embed another checker thus making checkers nested. Here is an example following the examples above.

```
checker ck1(irdy, trdy, frame_, event clk=$inferred_clock,
event reset = $inferred_disable);
default clocking @ clk; endclocking
default disable iff reset;
        property check1;
          irdy |-> ##2 trdy;
        endproperty
        property check2;
         $rose(irdy |=> frame_);
        endproperty
        checker ck2; //nested checker
                property check1;  //Redefinition of check1 within
                the local scope of checker ck2
                   $rose(trdy) |-> irdy;
                endproperty
                property check3;
                  $fell(irdy) |-> !frame_;
                endproperty
                checkp1: assert property check1;
                checkp3: assert property check3;
        checkp2: assert property check2;
        endchecker : ck2
ck2 ck2i; //instantiate ck2
endchecker : ck1
```

Points to note:

1. Checker ck1 properties are visible to checker ck2. Hence checker ck2 is able to 'assert' check2 of checker ck1.
2. Checker ck2 redefines property check1 for its local scope use. Since checker2 is instantiated in checker1, property check1 is not directly visible to checker check1. If you do want to access checker ck1's property check2, you will have to address it hierarchically as check1.check1.
3. The inferred clk and reset of checker ck1 are visible to checker ck2.

16.18.2 Checkers: Illegal Conditions

Following is *–not-* allowed in the checker body (this is as far as the author knowledge permits, since the simulators did not support checkers as of this writing to validate the following)

- A checker *cannot* be instantiated in a concurrent procedural construct such as fork..join, fork…join_any or fork…join_none.
- Continuous assignment.
- Procedural conditional and loop statements (if, case, for, etc.) are not allowed in checkers!
- Declaring nets in a checker body is illegal.
- Using blocking procedural assignments to checker variables is illegal. Such assignments can only be non-blocking.
- 'initial' procedural block may only contain concurrent, deferred and event control @. Nothing else.

- For example, following is illegal

```
checker myCheck;
    bit myBit;
    initial begin myBit=1'b1; //'initial' assignment to a variable  is I
    end
endchecker
```

We assigned a checker variable in the initial block – that is illegal.

Following will work

```
checker myCheck;
    bit myBit=1'b1;//This is Legal
endchecker
```

Following is illegal as well !

```
checker myCheck(a,b,c);
        bit myBit;
        ....
endchecker
module myMod;
        ...
        mycheck mck1(a,b,c);
        $display(mck1.myBit);//Hierarchical reference to variable is
                              //ILLEGAL
endmodule
```

- Following is illegal as well !!

```
checker myCheck(a,b,c);
    logic myBus[7:0];
    always @ (posedge clk) begin
    myBus[1:0] = 2'b0;
    myBus[7:1] = 6'b1;
          // Multiple assignments to the same variable is ILLEGAL. Bit
    // myBus[1] is common and assigned twice.
    end
endchecker
```

BUT the following is legal

```
checker myCheck(a,b,c);
    logic myBus[7:0];
    always @ (posedge clk) begin
    myBus[1:0] = 2'b0;
    myBus[7:2] = 6'b1; //Multiple assignments to bits of myBus is assigned
                       //only once.
    end
endchecker
```

- Following is illegal as well !!!

```
checker myCheck(bus,i);
        bit [3:0] bus, i;
        initial begin
        @ (posedge clk) i=0;
        bus[i]=3'b111;
        end
endchecker
module myMod
        logic [1:0] busIndex;
        logic [3:0] datafromBus;
        .....

myCheck m1 (datafromBus,busIndex);
//busIndex is non-constant ILLEGAL
myCheck m2(datafromBus,3'000); busIndex is constant -
endmodule
```

- Rule of thumb is that it is illegal to pass a non-constant index value to a checker variable which is used on the LHS of an assignment.
- Also note that if you instantiate a checker from a 'loop', the loop index cannot be used as actual for the checker variable.
- So, with all these restrictions on checker variable assignments what is one supposed to do? One of the solution is to use functions, as in the example below.

```
checker myCheck(a,b);
        bit a,b;
        initial begin
                @ (posedge clk);
                a=returnAvalue;
        end
function (bit a) returnAvalue;
         return a+1;
endfunction
endchecker
```

In this example, since we cannot assign a value to 'a' directly in the 'initial' block, we called the function 'returnAvalue' to accomplish the same. Note that 'a' is visible in the function 'returnAvalue'. Since function 'returnAvalue' is within the scope of checker mycheck, all the variables available in 'mycheck' are also visible in 'returnAvalue'. As evident, procedural control statements are allowed in a function.

16.18.3 Checkers: Important Points

1. Checker can only have inputs, no outputs.
2. A checker can be declared in a module, interface, program, checker (nested checkers), package, generate block and compilation unit scope.
3. 'type' and 'data' declarations are within the checker local scope and are static.
4. Clock and 'disable iff' contexts are inherited from the scope of the checker declaration.
5. You can modify/access DUT variables from a 'checker'! But my suggestion is to not overdo it. Checker code will not be portable and may result in spaghetti code. Try to keep a checker modular and reusable.
6. Checker formal argument cannot be of type 'local'.
7. Checker formal argument cannot be an 'interface' (note that a 'module' formal can be).
8. A checker body may contain the following elements (LRM 1800-2009).
    a. Declarations of 'let' constructs, sequences, properties and functions
    b. Deferred assertions
    c. Immediate and Concurrent assertions

i. A checker can contain only concurrent and deferred assertions. Immediate assertions are allowed only in the 'action' blocks of assertions and its final procedural blocks

d. Nested checkers
e. Covergroup declarations and assignments
f. Default clocking and disable iff declarations
g. Initial, always and final procedural blocks
h. Generate blocks, containing any of the above elements.
i. Similarly, an 'always' procedural block also may contain concurrent, deferred assertions, variable assignments and event control '@'. Nothing else.

9. The connectivity between the actual arguments and formal arguments of a checker follow exactly the same rules as those for modules, namely, positional association, explicit named association, implicit named association and wildcard name associations. Author leaves it to the reader to know of these techniques since they are age old like Verilog.
10. One or more covergroup declarations and/or instances are allowed in a checker. These covergroup declarations cannot appear in procedural code. Obviously, a covergroup can reference any variable visible in its scope. We will study covergroups under Functional Coverage chapter. Hence, I am deferring this theory for now.
11. Checker variables can be 'rand' (free variables).
12. The RHS of a checker variable assignment may contain the sequence method.triggered.

```
checker myCheck(a, b, c);

  …
  sequence busSeq;…; endsequence
  always @ (posedge clk) begin a <= busSeq.triggered; end

endchecker
```

16.18.4 Checker: Instantiation Rules

We have already covered Nested Checker rules. This section provides further guidelines on checker instantiation rules.

As noted above, a checker can be instantiated anywhere a concurrent assertion can be, except that a checker cannot be instantiated in a procedural construct such as fork..join, fork…join_any or fork…join_none. The mechanism for passing actual arguments to the formal arguments of a checker is the same as that for passing arguments to a property. It is important to note that it's the 'sampled' value

(i.e. the value in the preponed region) of an actual that is assigned to the formal of the checker (this rule is also the same as that for a property).

There is also a difference between a checker instantiation inside a procedural block and outside. Let us study this via an example (partially taken from LRM 1800-2009).

```
‘define MAX_SUM 256

checker c1(logic[7:0] a, b);
  logic [7:0] add;
  always @ (posedge clk) begin
      add <= a + 1’b1;
      p0: assert property (add < ‘MAX_SUM);
  end
p1: assert property (@ (posedge) clk add < ‘MAX_SUM);

p2: assert property (@ (posedge clk) clk a !=b);

endchecker

module m(input logic rst, clk, logic en, logic[7:0] in1, in2, in_array [20:0]);
c1 check_outside(in1, in2); //Concurrent (static) instantiation of ‘c1’ checker

always @ (posedge clk) begin
  automatic logic [7:0] v1 = 0;

  if (en) begin
        c1 check_inside(in1, v1); //Procedural instantiation of ‘c1’
  end

  for (int i = 0; i < 4; i++) begin
       v1 = v1+5;
    if (i !=2) begin
          c1 check_loop (in1, in_array [v1]); //Procedural (Loop) instantiation of ‘c1’
    end

  end
```

end

endmodule: m

Points to note in the above example

1. Each of the three instantiation of 'c1' (as noted in the example above) has its own copy of 'add'—which is rather obvious because without it, one instance of 'add' would clobber the 'add' of another instance.
2. 'p0' (in checker c1) will queue an evaluation for each of the three instances. These three instances of 'p0' will evaluate and report a violation during any time step when add is not less than MAX_SUM.
3. For check_loop, three procedural instances of 'p1' and 'p2' are queued (for I = 0,1,3) and they will evaluate at every posedge clk. Note that all instances of 'p1' will use the sampled value of 'add' and all instances of 'p2' will compare sampled value of 'in1' and 'in_array'
4. Since 'c1' (check_outside) instance is static (concurrent), the assertion statements in 'checker c1' are continually monitored and begin execution on any time step when their sampling edge (clock event) occur.

Please note: Checkers for Formal verification are not covered in this book since it is beyond the scope of the book. Specifically, 'assume property' is not explored beyond its context in simulation.

Chapter 17
SystemVerilog Assertions LABs

We will go through six simple labs that will solidify the practical features of properties and sequences. Each of this completely self-contained LAB is included on the server whose information is provided with the book. Each LAB includes, the DUT/Test-bench models, LAB Questions, 'run' scripts for both Linux and Windows and of course, the .solution directory with all required models so that you can simply execute the 'run' scripts and understand the results and answer the LAB questions.

17.1 LAB1: Assertions with/without Implication

Please note again that everything noted below (and for all the LABs) is provided on a server. You do not need to rewrite or copy/paste any of the following to run the LABs. The overall view of LAB objectives/questions is given here. Required run scripts/logs/etc. are on the server. The answers for each LAB are included in the .solution directory server. The answers are included in the book as well.

17.1.1 LAB1: 'bind' DUT Model and Test-Bench

****
LAB1 :: Objective
****

How to bind a design module to a property module that carries assertions for the design module.And further confirm your understanding of writing a property with/without implication (Fig. 17.1).

A. B. Mehta, *SystemVerilog Assertions and Functional Coverage*,
DOI: 10.1007/978-1-4614-7324-4_17,

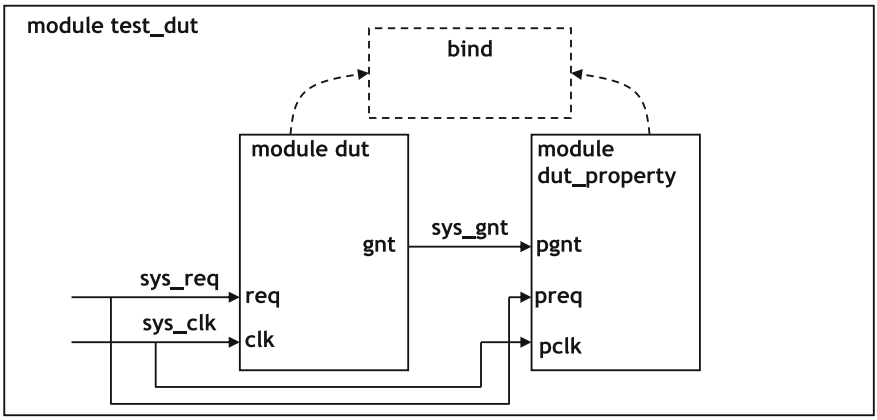


Fig. 17.1 LAB1: 'bind' assertions. Problem definition

****

LAB1 :: What you will do...

****

(1) 'bind' the design module 'dut' with its property module 'dut_property'
(2) Compile/simulate according to instructions given below.
(3) Study simulation log.
(4) Answer questions embedded in the simulation log file

****

LAB1 :: Database

****

FILES:

dut.v :: Verilog module that drives a simple req/gnt protocol.
dut_property.sv :: File that contains 'dut' properties/assertions.
test_dut.sv :: Test-bench for the 'dut'.
This is the file in which you'll 'bind' the 'dut'
with 'dut_property'

****

dut.v

****

```
/* Behavioral Verilog model that acts as the DUT driving asimple req/gnt
protocol*/

module dut(clk, req, gnt);
input logic clk,req;
output logic gnt;

initial
begin
  gnt=1'b0;
end
```

```
initial
begin
      @ (posedge req);
        @ (negedge clk); gnt=1'b0;
        @ (negedge clk); gnt=1'b1;
      @ (posedge req);
        @ (negedge clk); gnt=1'b0;
        @ (negedge clk); gnt=1'b0;
end
endmodule
```

****

dut_property.sv

****

```
module dut_property(pclk,preq,pgnt);
input pclk, preq, pgnt;

`ifdef no_implication
property pr1;
  @ (posedge pclk) preq ##2 pgnt;
endproperty
preqGnt: assert property (pr1) $display($stime,,,"\t\t %m PASS");
      else $display($stime,,,"\t\t %m FAIL");

`elsif implication
property pr1;
  @ (posedge pclk) preq |-> ##2 pgnt;
endproperty

preqGnt: assert property (pr1) $display($stime,,,"\t\t %m PASS");
      else $display($stime,,,"\t\t %m FAIL");

`elsif implication_novac
property pr1;
```

```
    @ (posedge pclk) preq |-> ##2 pgnt;
  endproperty
  preqGnt: assert property (pr1) else $display($stime,,,"\t\t %m FAIL");

  property pr2;
    @ (posedge pclk) preq ##2 pgnt;
  endproperty
  cpreqGnt: cover property (pr2) $display($stime,,,"\t\t %m PASS");
  `endif

  endmodule
```

17.1.2 LAB1: Questions

```
************************************************************
test_dut.sv
************************************************************
module test_dut;
bit sys_clk,sys_req;
wire sys_gnt;

/* Instantiate 'dut' */

dut dut1 (
            .clk(sys_clk),
            .req(sys_req),
            .gnt(sys_gnt)
      );

//-------------------------------------
// LAB EXERCISE - START
//-------------------------------------
//
```

```
// Add your code to bind 'dut' with 'dut_property' here.
// You need to know the names of the ports in the design as well as the
// property module to be able to bind them. So, here they are:

// Design module (dut.v)
// ----------------------
// module dut(clk, req, gnt);
//             input logic clk,req;
//             output logic gnt;

// Property module (dut_property.sv)
// ---------------------------------
//module dut_property(pclk,preq,pgnt);
//input pclk,preq,pgnt;

//--------------------------------------
// LAB EXERCISE - END
//--------------------------------------

always @ (posedge sys_clk)
  $display($stime,,,"clk=%b req=%b gnt=%b",sys_clk,sys_req,sys_gnt);

always #10 sys_clk = !sys_clk;

initial
begin
                      sys_req = 1'b0;
  @ (posedge sys_clk) sys_req = 1'b1; //30
  @ (posedge sys_clk) sys_req = 1'b0; //50
  @ (posedge sys_clk) sys_req = 1'b0; //70
  @ (posedge sys_clk) sys_req = 1'b1; //90
  @ (posedge sys_clk) sys_req = 1'b0; //110
  @ (posedge sys_clk) sys_req = 1'b0; //130

@ (posedge sys_clk);
@ (posedge sys_clk); $finish(2);
end
endmodule
```

```
************************************************************
LAB1 - Q U E S T I O N S (based on simulation log)
************************************************************

/* +define+no_implication

run -all
KERNEL:          10  clk=1 req=0 gnt=0
KERNEL:          10               test_implication FAIL
KERNEL:          30  clk=1 req=1 gnt=0
KERNEL:          50  clk=1 req=0 gnt=0
KERNEL:          50               test_implication FAIL
KERNEL:          70  clk=1 req=0 gnt=1
KERNEL:          70               test_implication FAIL

KERNEL:          70               test_implication PASS

            Q: WHY DOES THE PROPERTY FAIL -AND- PASS AT TIME (70) ??

KERNEL:          90  clk=1 req=1 gnt=0
KERNEL:         110  clk=1 req=0 gnt=0
KERNEL:         110               test_implication FAIL
KERNEL:         130  clk=1 req=0 gnt=0
KERNEL:         130               test_implication FAIL
KERNEL:         130               test_implication FAIL

            Q: WHY ARE THERE 2 failures AT TIME (130) ??
*/

/* +define+implication

run -all
KERNEL:          10  clk=1 req=0 gnt=0
KERNEL:          10               test_implication PASS
KERNEL:          30  clk=1 req=1 gnt=0
KERNEL:          50  clk=1 req=0 gnt=0
KERNEL:          50               test_implication PASS
KERNEL:          70  clk=1 req=0 gnt=1
KERNEL:          70               test_implication PASS
KERNEL:          70               test_implication PASS

            WHY ARE THERE 2 PASSes AT TIME 70 ??

KERNEL:          90  clk=1 req=1 gnt=0
KERNEL:         110  clk=1 req=0 gnt=0
KERNEL:         110               test_implication PASS
KERNEL:         130  clk=1 req=0 gnt=0
KERNEL:         130               test_implication FAIL
KERNEL:         130               test_implication PASS

            WHY IS THERE A PASS -and- a FAIL AT TIME 130 ??
*/

/* +define+implication_novac

run -all
KERNEL:          10  clk=1 req=0 gnt=0
KERNEL:          30  clk=1 req=1 gnt=0
```

```
KERNEL:          50  clk=1 req=0 gnt=0
KERNEL:          70  clk=1 req=0 gnt=1
KERNEL:          70                test_implication PASS
KERNEL:          90  clk=1 req=1 gnt=0
KERNEL:         110  clk=1 req=0 gnt=0
KERNEL:         130  clk=1 req=0 gnt=0
KERNEL:         130                test_implication FAIL

*/
```

17.2 LAB 2: Overlap and Non-Overlap Operators

17.2.1 LAB2 DUT Model and Test-Bench

****

LAB :: Objective

****

(1) Learn how property with overlapping implication operator works
(2) Learn how property with non-overlapping implication operator works
(3) Learn how pipelined threads work in SVA.

****

LAB :: Database

****

test_overlap_nonoverlap.sv :: This file contains the properties, sequences and the test-bench required to simulate the DUT.

****

test_overalp_nonoverlap.sv

****

```
module test_overlap_nonoverlap;

bit clk,cstart,req,gnt;


always @ (posedge clk)

  $display($stime,,, "clk=%b cstart=%b req=%b gnt=%b",clk,cstart,req,gnt);


always #10 clk = !clk;


sequence sr1;

  req ##2 gnt;

endsequence
```

```
`ifdef overlap
property pr1;
  @ (posedge clk) cstart |-> sr1;
endproperty

//Note that if a simulator supports filter on vacuous pass for a 'cover'
//the following property is not needed. You can simply use "property pr1"
//for 'cover' as well.
property pr1_for_cover;
  @ (posedge clk) cstart ##0 sr1;
endproperty

`elsif nonoverlap
property pr1;
  @ (posedge clk) cstart |=> sr1;
endproperty
//Note that if a simulator supports filter on vacuous pass for a 'cover'
//the property pr1_for_cover is not needed. You can simply use "property pr1"
//for 'cover' as well.
property pr1_for_cover;
  @ (posedge clk) cstart ##1 sr1;
endproperty
`endif

reqGnt: assert property (pr1) else $display($stime,,,"\t\t %m FAIL");
creqGnt: cover property (pr1_for_cover) $display($stime,,,"\t\t %m PASS");

initial
begin
  {cstart,req,gnt}=3'b000;
end

initial
```

```
begin
  @ (negedge clk); {cstart,req,gnt}=3'b100;
  @ (negedge clk); {cstart,req,gnt}=3'b110;
  @ (negedge clk); {cstart,req,gnt}=3'b000;
  @ (negedge clk); {cstart,req,gnt}=3'b001;
  @ (negedge clk); {cstart,req,gnt}=3'b110;
  @ (negedge clk); {cstart,req,gnt}=3'b110;
  @ (negedge clk); {cstart,req,gnt}=3'b111;
  @ (negedge clk); {cstart,req,gnt}=3'b010;
  @ (negedge clk); {cstart,req,gnt}=3'b000;
  @ (negedge clk); {cstart,req,gnt}=3'b001;
  @ (negedge clk); $finish(2);
end
endmodule
```

17.2.2 LAB2: Questions

```
*********************************************************
LAB Questions based on simulation log
*********************************************************
*************************************************************
Simulation Log - Q U E S  T I O N S
*************************************************************

/* +define+overlap

run -all
KERNEL:          10  clk=1 cstart=0 req=0 gnt=0
KERNEL:          30  clk=1 cstart=1 req=0 gnt=0
KERNEL:          30           test_overlap_nonoverlap FAIL

            Q: WHY DOES THE PROPERTY FAIL at 30?

KERNEL:          50  clk=1 cstart=1 req=1 gnt=0
KERNEL:          70  clk=1 cstart=0 req=0 gnt=0
KERNEL:          90  clk=1 cstart=0 req=0 gnt=1
KERNEL:          90           test_overlap_nonoverlap PASS
```

```
            Q: WHY DOES THE PROPERTY PASS at 90?

 KERNEL:         110  clk=1 cstart=1 req=1 gnt=0
 KERNEL:         130  clk=1 cstart=1 req=1 gnt=0
 KERNEL:         150  clk=1 cstart=1 req=1 gnt=1
 KERNEL:         150           test_overlap_nonoverlap PASS

            Q: WHY DOES THE PROPERTY PASS at 150?

KERNEL:         170  clk=1 cstart=0 req=1 gnt=0
KERNEL:         170            test_overlap_nonoverlap FAIL

            Q: WHY DOES THE PROPERTY FAIL at 170?

KERNEL:         190  clk=1 cstart=0 req=0 gnt=0
KERNEL:         190            test_overlap_nonoverlap FAIL

            Q: WHY DOES THE PROPERTY FAIL at 190?

KERNEL:         210  clk=1 cstart=0 req=0 gnt=1

*/

/* +define+nonoverlap

run -all
KERNEL:          10  clk=1 cstart=0 req=0 gnt=0
KERNEL:          30  clk=1 cstart=1 req=0 gnt=0
KERNEL:          50  clk=1 cstart=1 req=1 gnt=0
KERNEL:          70  clk=1 cstart=0 req=0 gnt=0
KERNEL:          70            test_overlap_nonoverlap FAIL

            Q: WHY DOES THE PROPERTY FAIL at 70?

KERNEL:          90  clk=1 cstart=0 req=0 gnt=1
KERNEL:          90            test_overlap_nonoverlap PASS


            Q: WHY DOES THE PROPERTY PASS at 90?

KERNEL:         110  clk=1 cstart=1 req=1 gnt=0
KERNEL:         130  clk=1 cstart=1 req=1 gnt=0
KERNEL:         150  clk=1 cstart=1 req=1 gnt=1
KERNEL:         170  clk=1 cstart=0 req=1 gnt=0
KERNEL:         170            test_overlap_nonoverlap FAIL

            Q: WHY DOES THE PROPERTY FAIL at 170?

KERNEL:         190  clk=1 cstart=0 req=0 gnt=0
KERNEL:         190            test_overlap_nonoverlap FAIL

            Q: WHY DOES THE PROPERTY FAIL at 190?

KERNEL:         210  clk=1 cstart=0 req=0 gnt=1
KERNEL:         210            test_overlap_nonoverlap PASS

            Q: WHY DOES THE PROPERTY PASS at 210?
*/
```

17.3 LAB3: FIFO Assertions

17.3.1 LAB3: DUT Model and Test-Bench

****
LAB3
****

We saw an example of an asynchronous FIFO in Sect. 14.1 and assertions thereof. For this LAB, I have chosen a simpler Synchronous FIFO for which you will exercise writing assertions. This way you will be familiar with writing assertions for both styles of FIFO. Note that one of the most important set of assertions that you may write for your project are the FIFO assertions. Like it or not, FIFOs always give trouble! (Fig. 17.2)

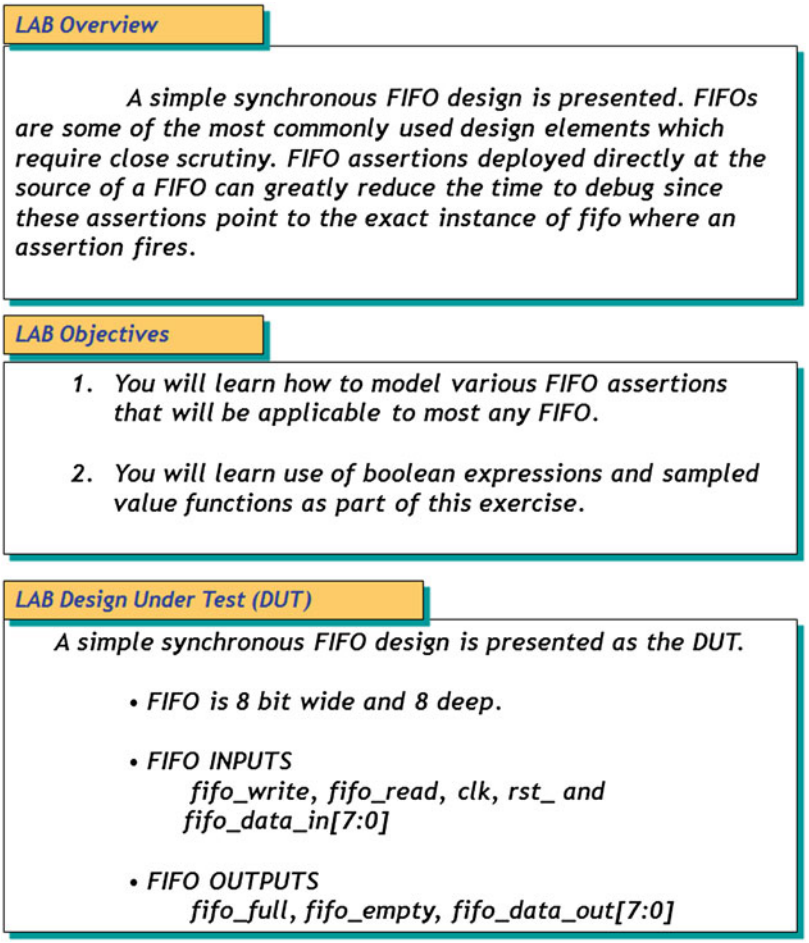
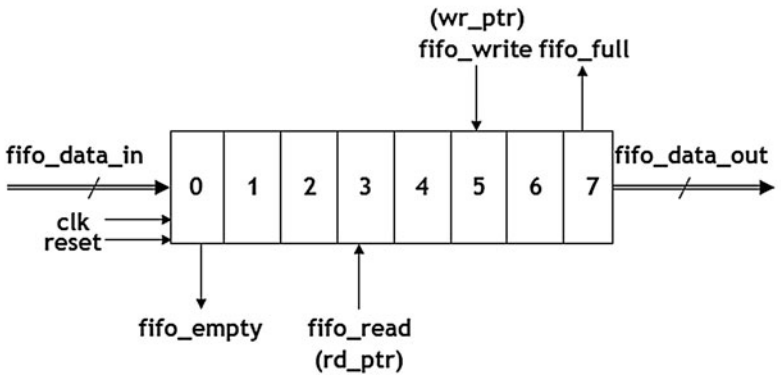


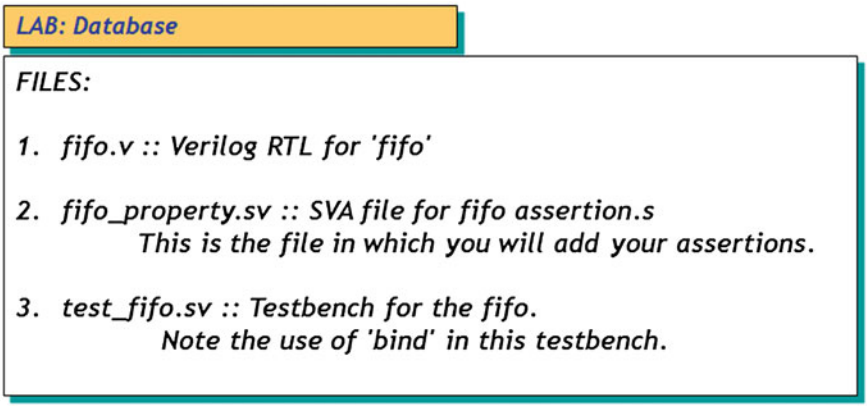
Fig. 17.2 LAB3: synchronous FIFO: problem definition

FIFO Specs

- *fifo maintains a wr_ptr and a rd_ptr*
  - *wr_ptr increments by 1 everytime a write is posted to the fifo on a fifo_write request*
  - *rd_ptr increments by 1 everytime a read is posted to the fifo on a fifo_read request*
- *fifo maintains a 'cnt' that increments on a write and decrements on a read. It is used to signal fifo_full and fifo_empty conditions as follows*
  - *When fifo 'cnt' is >= 7, fifo_full is asserted*
  - *When fifo 'cnt' is 0, fifo_empty is asserted.*



```
************************************************************
LAB3 :: Database
************************************************************
```



```
************************************************************
```

fifo.v

```
************************************************************

//`define fifo_depth 8
//`define fifo_width 8

module fifo
 (fifo_data_out,fifo_full,fifo_empty,fifo_write,fifo_read,clk,rst_,
            fifo_data_in);

parameter fifo_depth=8;
parameter fifo_width=8;

output logic [(fifo_width-1):0] fifo_data_out;
output logic fifo_full, fifo_empty;
input  logic fifo_write, fifo_read, clk, rst_;
input  logic [(fifo_width-1):0] fifo_data_in;

logic [(fifo_width-1):0] fifomem [0:(fifo_depth-1)];

logic [3:0] wr_ptr, rd_ptr;
logic [3:0] cnt;

always @ (posedge clk or negedge rst_)
  if (!rst_) begin
    rd_ptr  <= 0;
    wr_ptr  <= 0;
    cnt   <= 0;
`ifndef check1
    fifo_empty <= 1;
`endif
    fifo_full  <= 0;
  end
  else begin
    case ({fifo_write, fifo_read})
      2'b00: ;     // everyone's sleeping!
      2'b01: begin // read
       if (cnt>0) begin
                 rd_ptr <= rd_ptr + 1;
                 cnt  <= cnt  - 1;
               end
```

```
`ifdef check2
               if (cnt==0) fifo_empty <= 1;
`else
`ifdef check5
               if (cnt==1) fifo_empty <= 1;
              rd_ptr <= rd_ptr+1;
`else
               if (cnt==1) fifo_empty <= 1;
`endif
`endif
               fifo_full <= 0;
             end
      2'b10: begin // write
               if (cnt< fifo_depth) begin
                 fifomem[wr_ptr] <= fifo_data_in;
                 wr_ptr <= wr_ptr + 1;
                 cnt  <= cnt  + 1;
               end
`ifdef check3
               if (cnt>(fifo_depth-1)) fifo_full <= 1;
`else
`ifdef check4
               if (cnt>=(fifo_depth-1)) fifo_full <= 1;
              wr_ptr <= wr_ptr+1;
`else
               if (cnt>=(fifo_depth-1)) fifo_full <= 1;
`endif
`endif
               fifo_empty <= 0;
             end
      2'b11: // write && read
             //You cannot write if cnt is full; so read only
               if (cnt>(fifo_depth-1)) begin
                 rd_ptr  <= rd_ptr + 1;
                 cnt   <= cnt  - 1;
               end
            //You cannot read if cnt is empty; so write only
                    else if (cnt<1) begin
                    fifomem[wr_ptr] <= fifo_data_in;
                    wr_ptr  <= wr_ptr + 1;
```

```
                cnt   <= cnt  + 1;
              end
            //else write and read both
              else begin
                fifomem[wr_ptr] <= fifo_data_in;
                wr_ptr  <= wr_ptr + 1;
                rd_ptr  <= rd_ptr + 1;
              end
    endcase
  end

assign fifo_data_out = fifomem[rd_ptr];

endmodule
```

17.3.2 LAB3: Questions

LAB: Assertions to Code

Code assertions to check for the following conditions in the 'fifo' design.

CHECK # 1. Check that on reset
rd_ptr=0; wr_ptr=0; cnt=0; fifo_empty=1 and fifo_full=0

CHECK # 2. Check that fifo_empty is asserted when fifo 'cnt' is 0.
Disable this property 'iff (!rst)'

CHECK # 3. Check that fifo_full is asserted any time fifo 'cnt' is greater than 7.
Disable this property 'iff (!rst)'

CHECK # 4. Check that if fifo is full and you attempt to write (but not read) that the wr_ptr does not change.

CHECK # 5. Check that if fifo is empty and you attempt to read (but not write) that the rd_ptr does not change.

CHECK # 6. Write a property to Warn on write to a full fifo

CHECK # 7. Write a property to Warn on read from an empty fifo

****

LAB3: Questions – Assertion Questions embedded in the fifo_property.sv

****

I have provided the fifo_property.sv file. All you have to do is write your assertions in this file and simulate. I have coded '***dummy***' properties so that you can

compile the code. The .solution directory contains correct assertions and simulation log against which you can compare your results. Note that there is not just but one way to write an assertion and your assertion could look different from the one you see in the .solution directory. But the results must match with the simulation log in the .solution directory

```
`define rd_ptr test_fifo.fi1.rd_ptr
`define wr_ptr test_fifo.fi1.wr_ptr
`define cnt test_fifo.fi1.cnt

module fifo_property (
      input logic [7:0] fifo_data_out,
      input logic       fifo_full, fifo_empty,
      input logic       fifo_write, fifo_read, clk, rst_,
      input logic [7:0] fifo_data_in
                  );


parameter fifo_depth=8;
parameter fifo_width=8;



//        ------------------------------------------
//    1. Check that on reset,
//        rd_ptr=0; wr_ptr=0; cnt=0; fifo_empty=1 and fifo_full=0
//        ------------------------------------------

`ifdef check1
property check_reset;
  @ (posedge clk) !rst_ |-> `rd_ptr==0; //DUMMY... remove this line and
                                        //replace it with correct check
endproperty
check_resetP: assert property (check_reset) else $display($stime,"\t\t
FAIL::check_reset\n");
`endif
```

```
//      ----------------------------------------
//        2. Check that fifo_empty is asserted the same clock that fifo 'cnt'
//            is 0. Disable this property 'iff (!rst)'
//      ----------------------------------------

`ifdef check2
property fifoempty;
  @ (posedge clk) !rst_ |-> `rd_ptr==0; //DUMMY... remove this line and
                                        //replace it with correct check
endproperty
fifoemptyP: assert property (fifoempty) else $display($stime,"\t\t
FAIL::fifo_empty condition\n");
`endif


//      ----------------------------------------
//        3. Check that fifo_full is asserted any time fifo 'cnt'
//            is greater than 7. Disable this property 'iff (!rst)'
//      ----------------------------------------
`ifdef check3
property fifofull;
  @ (posedge clk) !rst_ |-> `rd_ptr==0; //DUMMY... remove this line and
                                        //replace it with correct check
endproperty
fifoemptyP: assert property (fifofull) else $display($stime,"\t\t
FAIL::fifo_empty condition\n");
`endif


//      ----------------------------------------
//        4. Check that if fifo is full and you attempt to write (but not read)
//            that the wr_ptr does not change.
//      ----------------------------------------

`ifdef check4
property fifo_full_write_stable_wrptr;
  @ (posedge clk) !rst_ |-> `rd_ptr==0; //DUMMY... remove this line and
                                        //replace it with correct check
endproperty
fifo_full_write_stable_wrptrP:              assert              property
(fifo_full_write_stable_wrptr)
        else    $display($stime,"\t\t    FAIL::fifo_full_write_stable_wrptr
condition\n");
`endif


`ifdef check5
```

```
//      ----------------------------------------
//      5. Check that if fifo is empty and you attempt to read (but not write)

//         that the rd_ptr does not change.
//      ----------------------------------------

property fifo_empty_read_stable_rdptr;
  @ (posedge clk) !rst_ |-> `rd_ptr==0; //DUMMY... remove this line and
                                        //replace it with correct check
endproperty
fifo_empty_read_stable_rdptrP: assert property (fifo_empty_read_stable_rdptr)

        else   $display($stime,   "\t\t   FAIL::fifo_empty_read_stable_rdptr
condition\n");
`endif

//      ----------------------------------------
//        6. Write a property to Warn on write to a full fifo
//      This property will give Warning with all simulations
//      ----------------------------------------

`ifdef check6
property write_on_full_fifo;
  @ (posedge clk) !rst_ |-> `rd_ptr==0; //DUMMY... remove this line and
                                        //replace it with correct check
endproperty
write_on_full_fifoP: assert property (write_on_full_fifo)
        else $display($stime,"\t\t WARNING::write_on_full_fifo\n");
`endif

//      ----------------------------------------
//        7. Write a property to Warn on read from an empty fifo
//      This property will give Warning with all simulations
//      ----------------------------------------

`ifdef check7
property read_on_empty_fifo;
  @ (posedge clk) !rst_ |-> `rd_ptr==0; //DUMMY... remove this line and
                                        //replace it with correct check
endproperty
read_on_empty_fifoP: assert property (read_on_empty_fifo)
     else $display($stime,"\t\t WARNING::read_on_empty_fifo condition\n");
`endif

endmodule
```

```
************************************************************
```

test_fifo.sv

```
************************************************************
module test_fifo;


wire  [7:0] fifo_data_out;

wire        fifo_full, fifo_empty;

logic       fifo_write, fifo_read, clk, rst_;

logic [7:0] fifo_data_in;


parameter fifo_depth = 8, fifo_width = 8;


fifo #(fifo_depth,fifo_width) fi1
(fifo_data_out,fifo_full,fifo_empty,fifo_write,fifo_read,clk,rst_,

                 fifo_data_in);


bind fifo fifo_property #(fifo_depth,fifo_width) fi1bind

      (fifo_data_out,fifo_full,fifo_empty,fifo_write,fifo_read,clk,rst_,fifo_
data_in);


initial

begin

  clk=0;

  fiforeset;

  fifowrite(10);

  fiforead(9);

  @ (posedge clk);

  @ (posedge clk);

  @ (posedge clk); $finish(2);

end


always #5 clk=!clk;

 task fiforeset;

   fifo_write=0; fifo_read=0; rst_=1;
```

```
  @ (negedge clk); rst_=0;
  @ (negedge clk);
  @ (negedge clk); rst_=1;
endtask

task fifowrite;
input int nwrite;
  fifo_read=0;
  for (int i=0; i<=nwrite-1; i++)
  begin
    @ (negedge clk); fifo_write=1; fifo_data_in=i;
      //$display($stime,,,"fifo Write Data = %0d",fifo_data_in);
  end
endtask

task fiforead;
input int nread;
  fifo_write=0;
  repeat(nread)
  begin
    @ (negedge clk); fifo_read=1;
      //$display($stime,,,"fifo Read Data = %0d",fifo_data_out);
  end
endtask

always @ (posedge clk)
  $display($stime,,,"rst_=%b clk=%b fifo_write=%b fifo_read=%b fifo_full=%b
fifo_empty=%b wr_ptr=%0d rd_ptr=%0d cnt=%0d",
      rst_,clk,fifo_write,fifo_read,fifo_full,fifo_empty,fi1.wr_ptr,fi1.rd_pt
r,fi1.cnt);

endmodule
```

17.4 LAB4: Counter

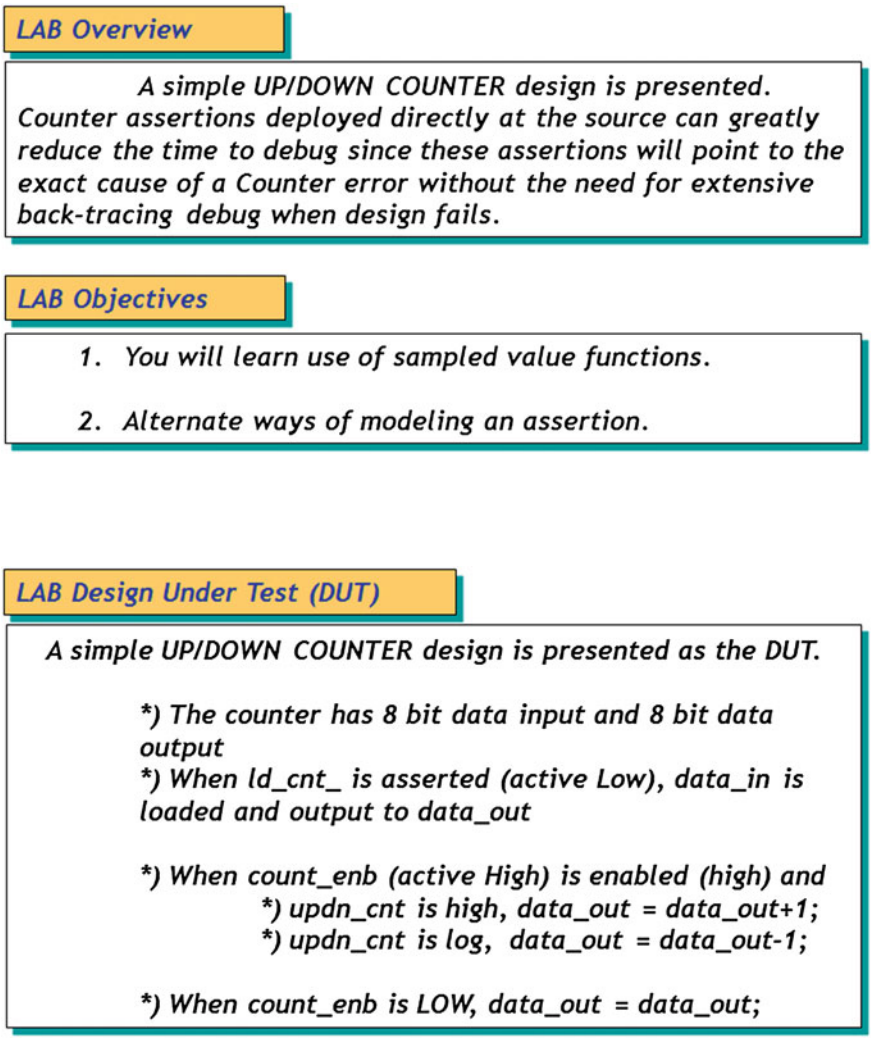


Fig. 17.3 LAB4 : counter : problem definition

LAB: Database

FILES:

1. counter.v :: Verilog RTL for a simple counter.

2. counter_property.sv :: SVA file for counter properties
   This is the file in which you will add your assertions.

3. test_counter.sv :: Testbench for the counter.
   Note the use of 'bind' in this testbench.

```
//////////////////////////////////////////////////////
counter.v
//////////////////////////////////////////////////////

module counter (
  input clk, rst_, ld_cnt_, updn_cnt, count_enb,
  input [7:0] data_in,
  output logic [7:0] data_out
  );

always @ (posedge clk or negedge rst_)
begin
  if (!rst_)
    begin
    `ifndef check1
       data_out <= 0;
    `endif
     end
  else
  begin

    //LOAD DATA
    if (!ld_cnt_)
      data_out <= data_in;

    //HOLD DATA
    `ifndef check2
     else if (!count_enb)
     data_out <= data_out;
    `endif

    //COUNT DATA
    `ifdef check3
    else
      case (updn_cnt)
        1'b1: data_out <= data_out - 1;
        1'b0: data_out <= data_out + 1;
      endcase
    `else
    else
      case (updn_cnt)
        1'b1: data_out <= data_out + 1;
        1'b0: data_out <= data_out - 1;
      endcase
    `endif

  end
end
endmodule
```

LAB: Assertions to Code

Code assertions to check for the following conditions in the 'counter' design.

CHECK # 1. Check that when 'rst_' is asserted (==0) that data_out == 8'b0

CHECK # 2. Check that if ld_cnt_ is deasserted (==1) and count_enb is not enabled (==0) that data_out HOLDS it's previous value.

Disable this property if rst is low.

CHECK # 3. Check that if ld_cnt_ is deasserted (==1) and count_enb is enabled (==1) that if updn_cnt==1 the count goes UP and if updn_cnt==0 the count goes DOWN.

Disable this property if rst is low.

17.4.1 LAB4: Questions

```
************************************************************
```

LAB4: Questions embedded in counter_property.sv

```
************************************************************
module counter_property (

  input clk, rst_, ld_cnt_, updn_cnt, count_enb,

  input [7:0] data_in,

  input logic [7:0] data_out

  );

//-------------------------------------

//     CHECK # 1. Check that when 'rst_' is asserted (==0) that

//     data_out == 8'b0

//-------------------------------------
```

```
`ifdef check1
property counter_reset;
  @ (posedge clk) data_in |=> data_out; // DUMMY - REMOVE this line and code
                                        // correct assertion
endproperty
counter_reset_check: assert property(counter_reset)
  else $display($stime,,,
                "\t\tCOUNTER RESET CHECK FAIL:: rst_=%b data_out=%0d \n",
                rst_,data_out);
`endif
//-------------------------------------
// CHECK # 2.Check that if ld_cnt_ is de-asserted (==1) and count_enb is not
// enabled (==0) that data_out HOLDS its previous value.
// Disable this property 'iff (!rst)'
//-------------------------------------

`ifdef check2
property counter_hold;
  @ (posedge clk) data_in |=> data_out; // DUMMY - REMOVE this line and code
                                        //correct assertion
endproperty

counter_hold_check: assert property(counter_hold)
  else $display($stime,,,"\t\tCOUNTER HOLD CHECK FAIL:: counter HOLD \n");
`endif
//-------------------------------------
//CHECK # 3. Check that if ld_cnt_ is de-asserted (==1) and count_enb is
//           enabled(==1) that if updn_cnt==1 the count goes UP and if
//           updn_cnt==0 the count goes DOWN.
//           Disable this property 'iff (!rst)'
//-------------------------------------
```

```
`ifdef check3
property counter_count;
  @ (posedge clk) data_in |=> data_out; // DUMMY - REMOVE this line and code
                                        //correct assertion
endproperty

counter_count_check: assert property(counter_count)
  else $display($stime,,,
            "\t\tCOUNTER COUNT CHECK FAIL:: UPDOWN COUNT using $past \n");
`endif

endmodule
```

test_counter.sv

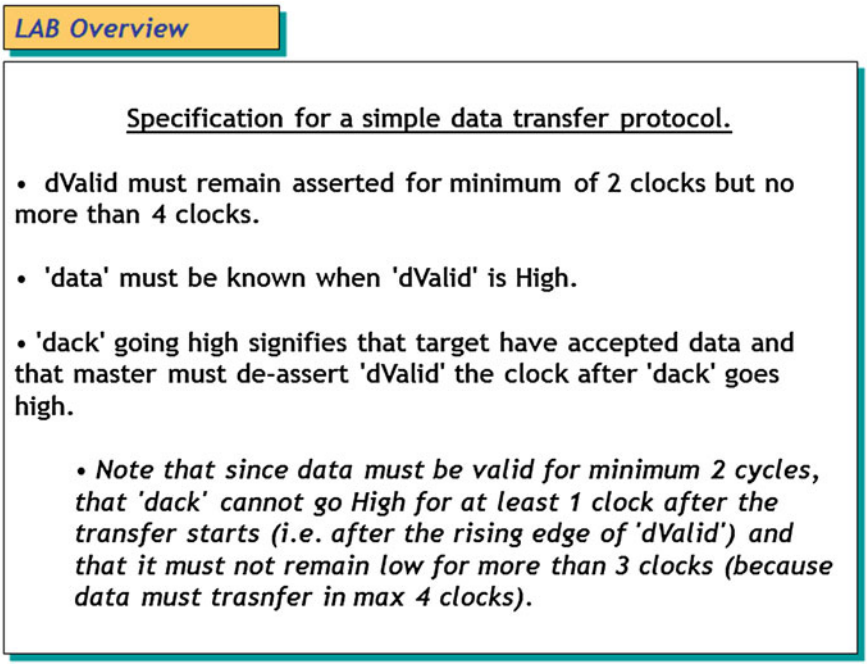
```
module test_counter;

logic clk, rst_, ld_cnt_, updn_cnt, count_enb;
logic [7:0] data_in;
wire [7:0] data_out;
int seed1;

counter  upc(
  clk, rst_, ld_cnt_, updn_cnt, count_enb,
  data_in,
  data_out
  );

bind counter counter_property bind_inst (
  clk, rst_, ld_cnt_, updn_cnt, count_enb,
  data_in,
  data_out
  );
```

```
initial

begin

  clk=1'b0;

  counter_init;

      count_up(100,10);

  repeat (2) @ (posedge clk);

      count_down(100,10);

  repeat (2) @ (posedge clk);

  @ (posedge clk); $finish(2);

end


always @ (posedge clk)

   $display($stime,,,"rst_=%b clk=%b count_enb=%b ld_cnt_=%b updn_cnt=%b
DIN=%0d DOUT=%0d",

   rst_, clk, count_enb, ld_cnt_, updn_cnt, data_in, data_out);


always #5 clk=!clk;


task counter_init;

  rst_=1'b1; ld_cnt_=1'b1; count_enb=1'b0; updn_cnt=1'b1;

  @ (negedge clk); rst_=1'b0;

  @ (negedge clk);

  @ (negedge clk); rst_=1'b1;

  @ (negedge clk); data_in=8'b0; ld_cnt_=1'b0;

  @ (negedge clk);

endtask


task count_up;

input logic [7:0] din;

input int count;

  @ (negedge clk); data_in=din; ld_cnt_=1'b0;

  @ (negedge clk); ld_cnt_=1'b1; count_enb=1'b1; updn_cnt=1'b1;

  repeat (count-1) @ (negedge clk);
```

```
  @ (negedge clk); count_enb=1'b0;
endtask

task count_down;
input logic [7:0] din;
input int count;
  @ (negedge clk); data_in=din; ld_cnt_=1'b0;
  @ (negedge clk); ld_cnt_=1'b1; count_enb=1'b1; updn_cnt=1'b0;
  repeat (count-1) @ (negedge clk);
  @ (negedge clk); count_enb=1'b0;
endtask

endmodule
```

17.5 LAB5: Data Transfer Protocol

(See Fig. 17.4)



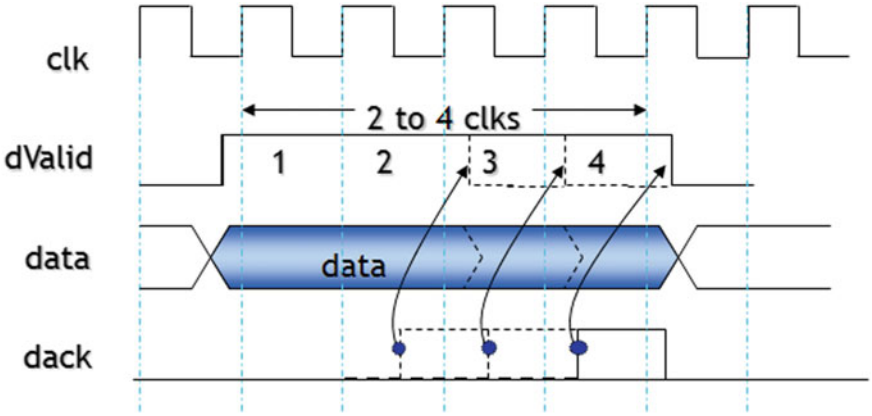


Fig. 17.4 LAB5: data transfer protocol : problem definition

LAB: Database

FILES:

1. *bus_protocol.v :: bus_protocol module that drive a simple bus protocol*
2. *bus_protocol_property.sv :: SVA file for bus_protocol assertions.*
   Note that this file is only an empty module shell.
   You will add properties that meet the specification described ablve.

3. *test_bus_protocol.sv :: Testbench for the bus_protocol module.*
   Note the use of 'bind' in this testbench.

LAB Objectives

Bus interfaces are common to any design and this lab will show you how to model assertions for common bus protocol specification.

You will learn

1. *Modeling temporal domain assertions for bus interface type logic.*
2. *Reinforce understanding of Edge sensitive and sampled value functions, consecutive repetition, boolean expressions, etc.*

LAB: Assertions to Code

Code assertions to check for the following conditions in the 'bus protocol' design.

CHECK # 1. Check that once dValid goes high that it is consecutively asserted (high) for minimum 2 and maximum 4 clocks

CHECK # 2. Check that data is not unknow and remains stable after dValid goes high and until dAck goes high.

CHECK # 3. Check that 'dAck' and 'dValid' relationship is maintained to complete the data transfer.

In other words,

'dack' going high signifies that target have accepted data and that master must de-assert 'dValid' the clock after 'dack' goes high.

Note that since data must be valid for minimum 2 cycles, that 'dack' cannot go High for at least 1 clock after the transfer starts (i.e. after the rising edge of 'dValid') and that it must not remain low for more than 3 clocks (because data must trasnfer in max 4 clocks).

17.5.1 LAB5: Questions

```
************************************************************
bus_protocol_property.sv : Questions embedded in the file
************************************************************

/* Properties (assertions) for bus_protocol.v

*/

module bus_protocol_property (input bit clk, dValid, dAck, reset,

                              input logic [7:0] data

);


   /*-------------------------------------------------

    CHECK # 1. Check that once dValid goes high that it is consecutively

    asserted (high) for minimum 2 and maximum 4 clocks.

    Check also that once dValid is asserted (high) for 2 to 4 clocks that

    it does de-assert (low) the very next clock.

    -------------------------------------------------*/

`ifdef check1

        property checkValid;

        @ (posedge clk) dValid |-> dValid; //DUMMY - REMOVE this line and
code

                                          //correct assertion

        endproperty

        assert property (checkValid) else

                                     $display($stime,,,"checkValid FAIL");

`endif
```

```
   /*-------------------------------------------------
    CHECK # 2. Check that data is not unknown and remains stable after
              dValid goes high and until dAck goes high.
   -------------------------------------------------*/


`ifdef check2
        property checkdataValid;
         @ (posedge clk) disable iff (reset)
         @ (posedge clk) dValid |-> dValid; //DUMMY - REMOVE this line and
                                            //code correct assertion
        endproperty
        assert property (checkdataValid) else
                                  $display($stime,,,"checkdataValid
FAIL");
`endif


 /*-------------------------------------------------
  CHECK # 3.
 'dack' going high signifies that target have accepted data and that master
  must de-assert 'dValid' the clock after 'dack' goes high.

  Note that since data must be valid for minimum 2 cycles, that 'dack' cannot

  go High for at least 1 clock after the transfer starts (i.e. after the
  rising edge of 'dValid')and that it must not remain low for more than 3
```

```
   clocks (because data must transfer in max 4 clocks).
  ----------------------------------------------------*/

`ifdef check3
      property checkdAck;
         @ (posedge clk) dValid |-> dValid; // DUMMY - REMOVE this line and code

                                          //correct assertion
      endproperty
      assert property (checkdAck) else $display($stime,,,"checkdAck FAIL");
`endif

 Endmodule

 ***********************************************************
 test_bus_protocol.v
 ***********************************************************
 module test_bus_protocol (output bit clk, reset,
                           input logic dValid, dAck,
                           input logic [7:0] data);

bus_protocol bp1(.*);
bind bus_protocol bus_protocol_property bpb1 (.*);

initial begin clk=1; reset=1; end
always #5 clk=!clk;

initial
begin
  @ (negedge clk); reset=1;
  @ (negedge clk); reset=0;
end

always @ (posedge clk)
  $display($stime,,,"clk=%b dValid=%b data=%h dAck=%b",
               clk,dValid,data,dAck);

endmodule
```

17.6 LAB6: PCI Read Protocol

LAB Overview

A simple system with a PCI Master and PCI Target modules designed to do a simple basic PCI Read operation.

The LAB shows how to derive and write simple but effective assertions for a PCI type bus.

(See Fig. 17.5)

LAB: Database

FILES:

pci_master.v :: A (very) simple PCI Master module driving only a simple Read cycle.
pci_target.v :: A (very) simple PCI Target module responding to a simple Read Cycle.
pci_protocol_property.v :: SVA file for PCI Read cycle assertions.

Note that this file is only an empty module shell. You will add properties that meet the specification described below.

test_pci_protocol.sv :: Testbench for the pci_protocol module.

LAB Objectives

1) Learn how to model temporal domain assertions for bus interface type logic.

2) Reinforce understanding of Edge sensitive sampled value functions, consecutive repetition, boolean expressions, etc.

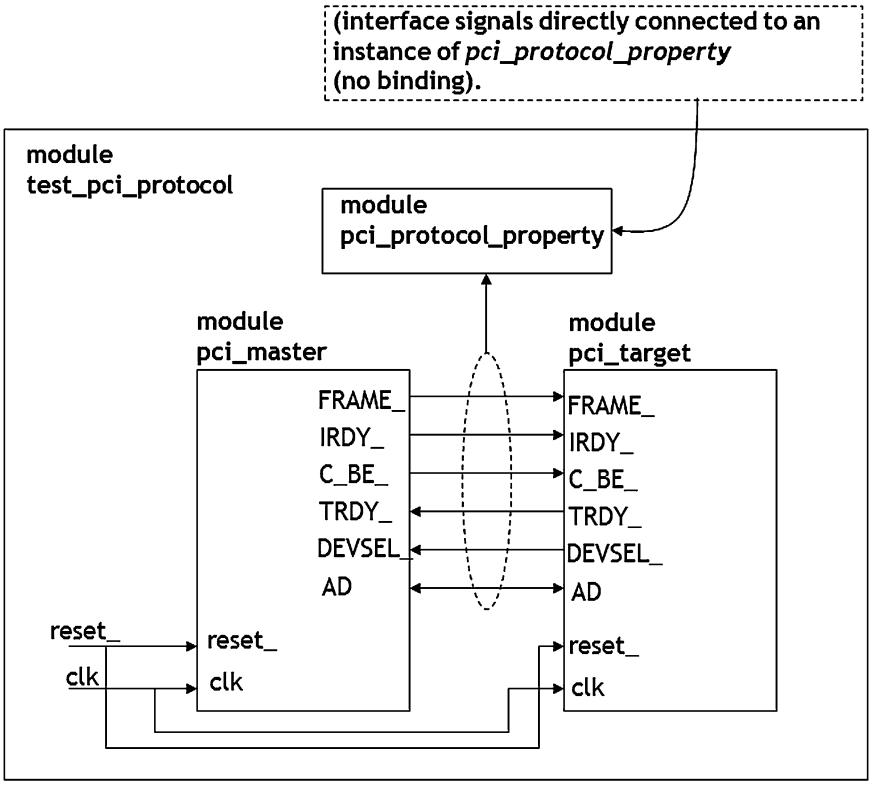
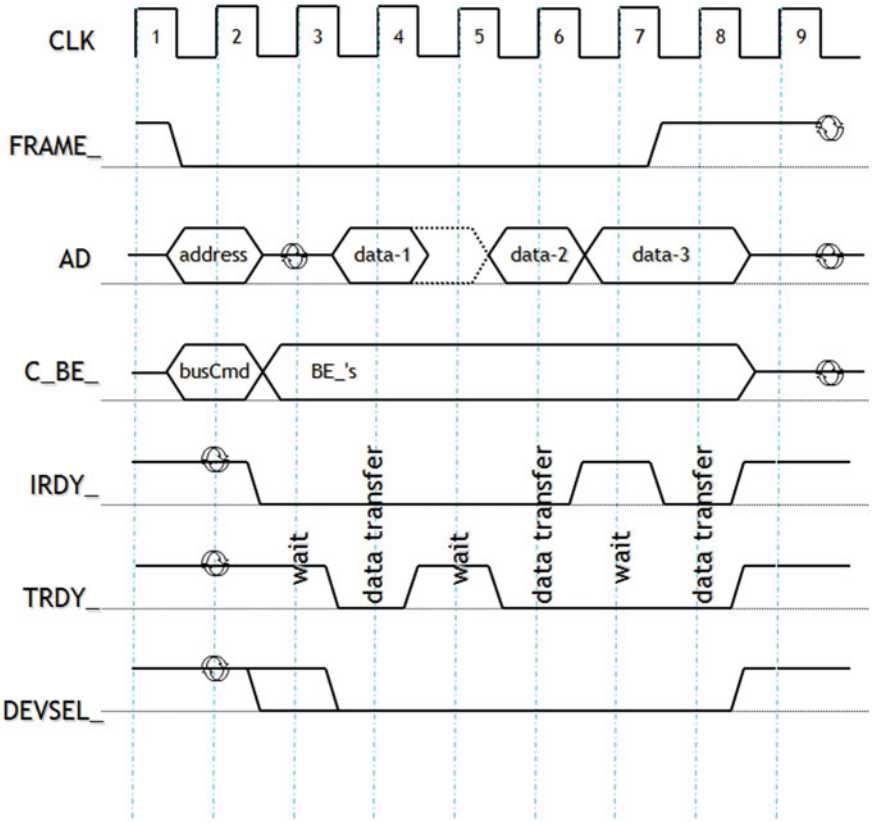


Fig. 17.5 LAB6: PCI protocol: problem definition



17.6.1 LAB6: Questions

LAB: Assertions to Code

Property Name	Description
checkPCI_AD_CBE (check1)	On falling edge of FRAME_, AD or C_BE_ bus cannot be unknown
checkPCI_DataPhase (check2)	When both IRDY_ and TRDY_ are asserted, AD or C_BE_ bus cannot be unknown
checkPCI_Frame_Irdy (check3)	FRAME can be de-asserted only if IRDY_ is asserted
checkPCI_trdyDevsel (check4)	TRDY_ can be asserted only if DEVSEL_ is asserted
checkPCI_CBE_during_trx (check5)	Once the cycle starts (i.e. at FRAME_ assertion) C_BE_ cannot float until FRAME_ is de-asserted.

```
************************************************************
```

pci_protocol_property.sv- LAB6 Questions embedded in code

```
************************************************************

module pci_protocol_property (input logic clk, reset_, TRDY_, DEVSEL_,
FRAME_,
                                          IRDY_,
                              input logic [3:0] C_BE_,
                              input logic [31:0] AD
);


  /*-------------------------------------------------
        CHECK # 1. On falling edge of FRAME_, AD or C_BE_
                   cannot be unknown.
    -------------------------------------------------*/
```

```
`ifdef check1
        property checkPCI_AD_CBE;
          @ (posedge clk) disable iff (!reset_)
            FRAME_ |-> 1'b1; //DUMMY -REMOVE this line and code correct
                            //assertion
        endproperty
        assert property (checkPCI_AD_CBE) else
$display($stime,,,"CHECK1:checkPCI_AD_CBE FAIL\n");
`endif
 /*-------------------------------------------------
  CHECK # 2. When IRDY_ and TRDY_ are asserted (low) AD
             or C_BE_ cannot be unknown.
  -------------------------------------------------*/
`ifdef check2
        property checkPCI_DataPhase;
          @ (posedge clk) disable iff (!reset_)
            FRAME_ |-> 1'b1; // DUMMY - REMOVE this line and code correct
                            //assertion
        endproperty
        assert property (checkPCI_DataPhase) else
$display($stime,,,"CHECK2:checkPCI_DataPhase FAIL\n");
`endif
/*-------------------------------------------------
CHECK # 3. FRAME_ can go High only if IRDY_ is asserted.
           In other words, master can signify end of cycle
           only if IRDY_ is asserted.
-------------------------------------------------*/
`ifdef check3
        property checkPCI_Frame_Irdy;
          @ (posedge clk) disable iff (!reset_)
            FRAME_ |-> 1'b1; // DUMMY - REMOVE this line and code correct
                            //assertion
        endproperty
```

```
        assert property (checkPCI_Frame_Irdy) else
 $display($stime,,,"CHECK3:checkPCI_frmIrdy FAIL\n");

 `endif


 /*-----------------------------------------------------
  CHECK # 4. TRDY_ can be asserted (low) only if DEVSEL_
             is asserted (low)
  -----------------------------------------------------*/


 `ifdef check4
        property checkPCI_trdyDevsel;
          @ (posedge clk) disable iff (!reset_)
            FRAME_ |-> 1'b1; // DUMMY - REMOVE this line and code correct
                             //assertion
        endproperty
        assert property (checkPCI_trdyDevsel) else
 $display($stime,,,"CHECK4:checkPCI_trdyDevsel FAIL\n");
 `endif
/*-----------------------------------------------------
 CHECK # 5. Once the cycle starts (i.e. at FRAME_ assertion)
            C_BE_ should not float until FRAME_ is de-asserted
 -----------------------------------------------------*/


`ifdef check5
       property checkPCI_CBE_during_trx;
         @ (posedge clk) disable iff (!reset_)
           FRAME_ |-> 1'b1; // DUMMY - REMOVE this line and code correct
                            //assertion
       endproperty
       assert property (checkPCI_CBE_during_trx) else
$display($stime,,,"CHECK5:checkPCI_CBE_during_trx FAIL\n");

`endif

endmodule
```

Chapter 18
System Verilog Assertions: LAB Answers

18.1 LAB1: Answers : 'Bind' and Implication Operators (Figs. 18.1, 18.2, 18.3)

LAB 1 : Code snippet from test_dut.sv showing 'bind' between 'dut' and 'dut_property'

```
bind dut dut_property dut_bind_inst (
            .pclk(clk),
            .preq(req),
            .pgnt(gnt)
      );
```

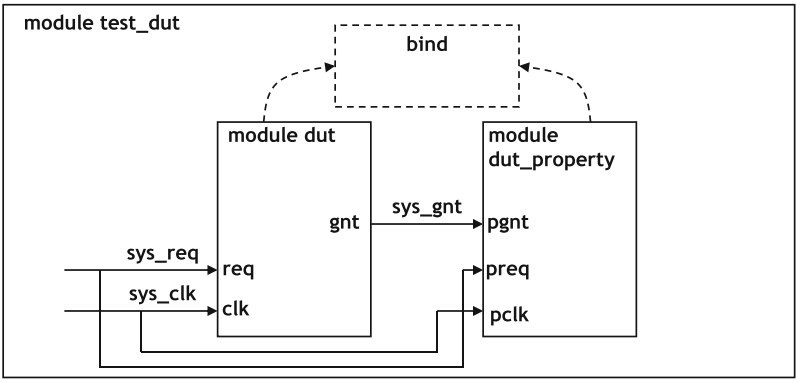


Fig. 18.1 LAB1: 'bind' assertions (answers)

A. B. Mehta, *SystemVerilog Assertions and Functional Coverage*,
DOI: 10.1007/978-1-4614-7324-4_18,

LAB 1 : Code snippet for "no_implication"

```
property pr1;
  @(posedge clk) req ##2 gnt;
endproperty
reqGnt: assert property (pr1) $display($stime,,,"\t\t  %m PASS");
              else $display($stime,,,"\t\t  %m FAIL");
```

LAB 1 : Q&A on "no_implication"

```
/* +define+no_implication

run -all
KERNEL:       10  clk=1 req=0 gnt=0
KERNEL:       10            test_implication FAIL
KERNEL:       30  clk=1 req=1 gnt=0
KERNEL:       50  clk=1 req=0 gnt=0
KERNEL:       50            test_implication FAIL
KERNEL:       70  clk=1 req=0 gnt=1
KERNEL:       70            test_implication FAIL
KERNEL:       70            test_implication PASS

             Q: WHY IS THERE A FAIL -AND- A PASS AT TIME (70) ??

             A: The FAIL at 70 is for the thread starting at time 70.
               At 70, req==0 and since there is no implication, the property fails
               because without an implication there is no antecedent to match before
               the check begins. Whenever at posedge clk, 'req' is detected low,
                the property will fail.

               The PASS at 70 is for the thread that starts at 30.
               At 30, req==1, so property eval proceeds.
               At 70 (i.e. 2 clocks later) gnt==1 as required by the property and the
               property PASSes.
```

Fig. 18.2 LAB1: Q&A on 'no_implication' operator (answers)

LAB 1 : Code snippet for "no_implication"

```
property pr1;
  @(posedge clk) req ##2 gnt;
endproperty
reqGnt: assert property (pr1) $display($stime,,,"\t\t  %m PASS");
              else $display($stime,,,"\t\t  %m FAIL");
```

LAB 1 : Q&A on "no_implication"

```
KERNEL:       90  clk=1 req=1 gnt=0
KERNEL:      110  clk=1 req=0 gnt=0
KERNEL:      110            test_implication FAIL
KERNEL:      130  clk=1 req=0 gnt=0
KERNEL:      130            test_implication FAIL
KERNEL:      130            test_implication FAIL

            Q: WHY ARE THERE 2 FAILs AT TIME (130) ??

            A: The first failures is for the thread starting at time 90
              At 90, req==1, so property eval proceeds.
              At 130 (i.e. 2 clocks later) gnt==0 which violates the property and the
              property FAILs.

              The second failure is for the thread starting at time 130.
              At 130, req==0 and since there is no implication, the property fails
              because without an implication there is no antecedent to match before
              the check begins. Whenever at posedge clk, 'req' detected low,
               the property will fail.
```

Fig. 18.2 (continued)

LAB 1 : Code snippet for "implication"

```
property pr1;
  @(posedge clk) req |-> ##2 gnt;
endproperty

reqGnt: assert property (pr1) $display($stime,,,"\t\t  %m PASS");
             else $display($stime,,,"\t\t  %m FAIL");
```

LAB 1 : Q&A on "implication"

```
run -all
KERNEL:       10  clk=1 req=0 gnt=0
KERNEL:       10            test_implication PASS
KERNEL:       30  clk=1 req=1 gnt=0
KERNEL:       50  clk=1 req=0 gnt=0
KERNEL:       50            test_implication PASS
KERNEL:       70  clk=1 req=0 gnt=1
KERNEL:       70            test_implication PASS
KERNEL:       70            test_implication PASS

              Q: WHY ARE THERE 2 PASSes AT TIME 70 ??

              A: The first pass is for the thread starting at time 30.
                 At 30, req==1, so property eval proceeds.
                 At 70 (i.e. 2 clocks later) gnt==1 as required by the property and the
                 property PASSes.

                 The second pass is for the thread starting at time 70.
                 At 70, req==0 and since there is implication, the consequent eval won't
                 start. However, there is a PASS action_block associated with the
                 property which triggers because of the vacuous pass phenomenon. In
                 other wods, whenever 'req' is low, the antecedent won't match and the
                 property will pass vacuosly.
```

Fig. 18.3 LAB1: Q&A on 'implication' operator (answers)

LAB 1 : Code snippet for "implication"

```
property pr1;
  @(posedge clk) req |-> ##2 gnt;
endproperty

reqGnt: assert property (pr1) $display($stime,,,"\t\t  %m PASS");
              else $display($stime,,,"\t\t  %m FAIL");
```

LAB 1 : Q&A on "implication"

```
KERNEL:       90  clk=1 req=1 gnt=0
KERNEL:      110  clk=1 req=0 gnt=0
KERNEL:      110            test_implication PASS
KERNEL:      130  clk=1 req=0 gnt=0
KERNEL:      130            test_implication FAIL
KERNEL:      130            test_implication PASS

            Q: WHY IS THERE A PASS -and- a FAIL AT TIME 130 ??

            A: The failure is for the thread starting at time 90.
              At 90, req==1, so property eval proceeds.
              At 130 (i.e. 2 clocks later) gnt==0 which violates the property and the
              property FAILs.

              The pass is for the property stating at 130.
              At 130, req==0 and since there is implication, the consequent eval won't
              start. However, there is a PASS action_block associated with the
              property which triggers because of the vacuous pass phenomenon. In
              other words, whenever 'req' is low, the antecedent won't match and the
              property will pass vacuosly.
```

Fig. 18.3 (continued)

18.2 LAB2: Answers : Overlap and Non-Overlap Operators (Figs. 18.4, 18.5)

LAB 2 : Code snippet with "overlap" operator

```
sequence sr1;
  req ##2 gnt;
endsequence

property pr1;
  @(posedge clk) cstart |-> sr1;
endproperty

property pr1_for_cover;
  @(posedge clk) cstart ##0 sr1;
endproperty
```

LAB 2 : Q&A on "overlap" operator

```
run -all
KERNEL:       10  clk=1 cstart=0 req=0 gnt=0
KERNEL:       30  clk=1 cstart=1 req=0 gnt=0
KERNEL:       30            test_overlap_nonoverlap FAIL

          Q: WHY DOES THE PROPERTY FAIL at 30?

            A: At time 30, cstart=1; so antecedent matches and consequent eval starts
              At time 30, req is NOT equal to 1 as required by overlapping implication
              and the consequent fails right away and the property FAILs.

KERNEL:       50  clk=1 cstart=1 req=1 gnt=0
KERNEL:       70  clk=1 cstart=0 req=0 gnt=0
KERNEL:       90  clk=1 cstart=0 req=0 gnt=1
KERNEL:       90            test_overlap_nonoverlap PASS

          Q: WHY DOES THE PROPERTY PASS at 90?

            A: At time 50, cstart=1; so antecedent matches and consequent eval starts
              At time 50 (i.e, the same clock as required by overlapping implication),
              req=1; so consequent eval continues
              At time 70, gnt=1 as required by the property and the consequent
              matches and the property PASSes.
```

Fig. 18.4 LAB1: Q&A on 'overlap' operator (answers)

LAB 2 : Q&A on "overlap" operator

```
KERNEL:      110  clk=1 cstart=1 req=1 gnt=0
KERNEL:      130  clk=1 cstart=1 req=1 gnt=0
KERNEL:      150  clk=1 cstart=1 req=1 gnt=1
KERNEL:      150          test_overlap_nonoverlap PASS

          Q: WHY DOES THE PROPERTY PASS at 150?

            A: At time 110, cstart=1; antecedent matches and consequent eval starts.
               At time 110 (i.e, the same clock as required by overlapping
               implication), req=1; so consequent eval continues
               At time 150 (i.e 2 clocks after 110), gnt=1 as required by the property
               so the consequent matches and the property PASSes

KERNEL:      170  clk=1 cstart=0 req=1 gnt=0
KERNEL:      170          test_overlap_nonoverlap FAIL

          Q: WHY DOES THE PROPERTY FAIL at 170?

            A: At time 130, cstart=1;antecedent matches and consequent eval starts
              At time 130 (i.e, the same clock as required by overlapping implication),
              req=1; so consequent eval continues
              At time 170 (i.e 2 clocks after 130), gnt is NOT equal to 0 as required by
              the property so the consequent does not match and the property FAILs

KERNEL:      190  clk=1 cstart=0 req=0 gnt=0
KERNEL:      190          test_overlap_nonoverlap FAIL

          Q: WHY DOES THE PROPERTY FAIL at 190?

            A: At time 150, cstart=1; antecedent matches and consequent eval starts
              At time 150 (i.e, the same clock as required by overlapping implication),
              req=1; so consequent eval continues
              At time 190 (i.e 2 clocks after 150), gnt is NOT equal 0 as required by
              the property so the consequent does not match and the property FAILs
```

Fig. 18.4 (continued)

LAB 2 : Code snippet with "non-overlap" operator

```
sequence sr1;
  req ##2 gnt;
endsequence

property pr1;
  @(posedge clk) cstart |=> sr1;
endproperty

property pr1_for_cover;
  @(posedge clk) cstart ##1 sr1;
endproperty
```

LAB 2 : Q&A on "non-overlap" operator

```
KERNEL:      10  clk=1 cstart=0 req=0 gnt=0
KERNEL:      30  clk=1 cstart=1 req=0 gnt=0
KERNEL:      50  clk=1 cstart=1 req=1 gnt=0
KERNEL:      70  clk=1 cstart=0 req=0 gnt=0
KERNEL:      70            test_overlap_nonoverlap FAIL

          Q: WHY DOES THE PROPERTY FAIL at 70?

            A: This failure is for the thread that started at time 50 (and not 30).
              At time 50, cstart=1; so antecedent matches and consequent eval starts
              At time 70 (i.e, one clock later as required by nonoverlapping
              implication), req is NOT EQUAL to 1; so consequent does not match and
              the property FAILs

KERNEL:      90  clk=1 cstart=0 req=0 gnt=1
KERNEL:      90            test_overlap_nonoverlap PASS

          Q: WHY DOES THE PROPERTY PASS at 90?

            A: This pass is for the thread that started at time 30 (and not 50).
              At time 30, cstart=1; so antecedent matches and consequent eval starts
              At time 50 (i.e, one clock later as required by nonoverlapping
              implication), req == 1; so consequent eval continues
              At time 90 (i.e, two clocks later as required by the property),
              gnt == 1; so consequent matches and the property PASSes.
```

Fig. 18.5 LAB1: Q&A on 'non-overlap' operator (answers)

LAB 2 : Q&A on "non-overlap" operator

```
KERNEL:     110  clk=1 cstart=1 req=1 gnt=0
KERNEL:     130  clk=1 cstart=1 req=1 gnt=0
KERNEL:     150  clk=1 cstart=1 req=1 gnt=1
KERNEL:     170  clk=1 cstart=0 req=1 gnt=0
KERNEL:     170          test_overlap_nonoverlap FAIL

          Q: WHY DOES THE PROPERTY FAIL at 170?

            A: This failure is for the thread that started at time 110
              At time 110, cstart=1; antecedent matches and consequent eval starts
              At time 130 (i.e, one clock later as required by nonoverlapping
              implication), req is EQUAL to 1; so consequent eval continues.
              At time 170 (i.e, two clocks later as required by the property),
              gnt is NOT EQUAL to 1; so consequent does not match and
              the property FAILs.

KERNEL:     190  clk=1 cstart=0 req=0 gnt=0
KERNEL:     190          test_overlap_nonoverlap FAIL

          Q: WHY DOES THE PROPERTY FAIL at 190?

            A: This failure is for the thread that started at time 130
              At time 110, cstart=1; so antecedent matches and consequent eval starts
              At time 150 (i.e, one clock later as required by nonoverlapping
              implication), req is EQUAL to 1; so consequent eval continues.
              At time 190 (i.e, two clocks later as required by the property),
              gnt is NOT EQUAL to 1; so consequent does NOT match and
              the property FAILs.

KERNEL:     210  clk=1 cstart=0 req=0 gnt=1
KERNEL:     210          test_overlap_nonoverlap PASS

          Q: WHY DOES THE PROPERTY PASS at 210?

            A: This pass is for the thread that started at time 150
              At time 150, cstart=1; antecedent matches and consequent eval starts
              At time 170 (i.e, one clock later as required by nonoverlapping
              implication), req is EQUAL to 1; so consequent eval continues.
              At time 210 (i.e, two clocks later as required by the property),
              gnt is EQUAL to 1; so consequent matches and the property PASSes.
```

Fig. 18.5 (continued)

18.3 LAB3: Answers : FIFO (Fig. 18.6)

LAB 3 : fifo_property.sv

```
//     ------------------------------------------
//       1. Check that on reset,
//                rd_ptr=0; wr_ptr=0; cnt=0; fifo_empty=1 and fifo_full=0
//     ------------------------------------------
`ifdef check1
property check_reset;
  @(posedge clk)
    (!rst_ |-> (`rd_ptr==0 && `wr_ptr==0 && fifo_empty==1 && fifo_full==0));
endproperty
check_resetP: assert property (check_reset) else $display($stime,"\t\t
FAIL::check_reset\n");
`endif

//     ------------------------------------------
//       2. Check that fifo_empty is asserted the same clock that fifo 'cnt' is 0.
//          Disable this property 'iff (!rst)'
//     ------------------------------------------
`ifdef check2
property fifoempty;
  @(posedge clk) disable iff (!rst_)
    (`cnt==0 |-> fifo_empty);
endproperty
fifoemptyP: assert property (fifoempty) else $display($stime,"\t\t
FAIL::fifo_empty condition\n");
`endif

//     ------------------------------------------
//       3. Check that fifo_full is asserted any time fifo 'cnt' is greater than 7.
//          Disable this property 'iff (!rst)'
//     ------------------------------------------
`ifdef check3
property fifofull;
  @(posedge clk) disable iff (!rst_)
    (`cnt>(fifo_depth-1)  |-> fifo_full);
endproperty
fifofullP: assert property (fifofull) else $display($stime,"\t\t FAIL::fifo_full
condition\n");
`endif
```

Fig. 18.6 LAB3: FIFO: Answers

LAB 3 : fifo_property.sv

```
//     ------------------------------------------
//       4. Check that if fifo is full and you attempt to write (but not read) that
//          the wr_ptr does not change.
//     ------------------------------------------
`ifdef check4
property fifo_full_write_stable_wrptr;
  @(posedge clk) disable iff (!rst_)
    (fifo_full && fifo_write && !fifo_read |=> $stable(`wr_ptr));
endproperty
fifo_full_write_stable_wrptrP: assert property (fifo_full_write_stable_wrptr)
    else $display($stime,"\t\t FAIL::fifo_full_write_stable_wrptr condition\n");
`endif

`ifdef check5
//     ------------------------------------------
//       5. Check that if fifo is empty and you attempt to read (but not write) that
//          the rd_ptr does not change.
//     ------------------------------------------
property fifo_empty_read_stable_rdptr;
  @(posedge clk) disable iff (!rst_)
    (fifo_empty && fifo_read && !fifo_write |=> $stable(`rd_ptr));
endproperty
fifo_empty_read_stable_rdptrP: assert property (fifo_empty_read_stable_rdptr)
              else $display($stime,"\t\t FAIL::fifo_empty_read_stable_rdptr
condition\n");
`endif

//     ------------------------------------------
//       6. Write a property to Warn on write to a full fifo
//             This property will give Warning with all simulations
//     ------------------------------------------
`ifdef check6
property write_on_full_fifo;
  @(posedge clk) disable iff (!rst_)
    fifo_full |-> !fifo_write;
endproperty
write_on_full_fifoP: assert property (write_on_full_fifo)
              else $display($stime,"\t\t WARNING::write_on_full_fifo\n");
`endif
```

Fig. 18.6 (continued)

LAB 3 : fifo_property.sv

```
//     ----------------------------------------
//       7. Write a property to Warn on read from an empty fifo
//             This property will give Warning with all simulations
//     ----------------------------------------
`ifdef check7
property read_on_empty_fifo;
  @(posedge clk) disable iff (!rst_)
    fifo_empty |-> !fifo_read;
endproperty
read_on_empty_fifoP: assert property (read_on_empty_fifo)
          else $display($stime,"\t\t  WARNING::read_on_empty_fifo  condition\n");
`endif
```

Fig. 18.6 (continued)

18.4 LAB4: Answers : Counter (Fig. 18.7)

LAB 4 : counter_property.sv

```
//-------------------------------------
//       CHECK # 1. Check that when 'rst_' is asserted (==0) that data_out == 8'b0
//-------------------------------------
`ifdef check1
property counter_reset;
  @(clk) disable iff (rst_) !rst_ |=> (data_out == 8'b0);
endproperty

counter_reset_check: assert property(counter_reset)
  else $display($stime,,,"\t\tCOUNTER  RESET CHECK FAIL:: rst_=%b data_out=%0d \n",
                                                    rst_,data_out);
`endif

//-------------------------------------
//       CHECK # 2. Check that if ld_cnt_ is deasserted (==1) and count_enb is not enabled
//                (==0) that data_out HOLDS it's previous value.
//                Disable this property 'iff (!rst)'
//-------------------------------------
`ifdef check2
property counter_hold;
  @(posedge clk) disable iff (!rst_) (ld_cnt_ & !count_enb) |=> data_out ===
$past(data_out);
endproperty

counter_hold_check: assert property(counter_hold)
  else $display($stime,,,"\t\tCOUNTER  HOLD CHECK FAIL:: counter HOLD \n");
`endif
```

Fig. 18.7 LAB4: Counter : Answers

LAB 4 : counter_property.sv

```
`ifdef check3
property counter_count;
 @(posedge clk) disable iff (!rst_) (ld_cnt_ & count_enb) |->
   if (updn_cnt) ##1 (data_out-8'h01) == $past(data_out)
   else          ##1 (data_out+8'h01) == $past(data_out);
endproperty

counter_count_check: assert property(counter_count)
 else $display($stime,,,"\t\tCOUNTER  COUNT CHECK FAIL::UPDOWN COUNT using $past \n");
`endif

//-------------------------------------
// Alternate way of writing assertion for CHECK # 3
// Check for count using local variable
//-------------------------------------
/*
`ifdef check3
property counter_count_local;
logic[7:0] local_data;
 @(posedge clk) disable iff (!rst_) (ld_cnt_ & count_enb, local_data = data_out) |->
   if (updn_cnt) ##1 (data_out == (local_data+8'h01))
   else          ##1 (data_out == (local_data-8'h01));
endproperty

counter_count_check: assert property(counter_count)
 else $display($stime,,,"\t\tCOUNTER  COUNT CHECK FAIL:: UPDOWN COUNT using $past
\n");

`endif
*/
```

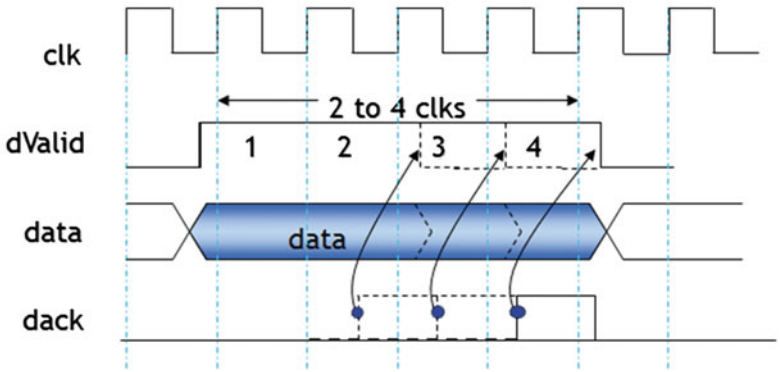
Fig. 18.7 (continued)

18.5 LAB5: Answers : Data Transfer Protocol (Fig. 18.8)

LAB Overview

Specification for a simple data transfer protocol.

- dValid must remain asserted for minimum of 2 clocks but no more than 4 clocks.
- 'data' must be known when 'dValid' is High.
- 'dack' going high signifies that target have accepted data and that master must de-assert 'dValid' the clock after 'dack' goes high.
  - *Note that since data must be valid for minimum 2 cycles, that 'dack' cannot go High for at least 1 clock after the transfer starts (i.e. after the rising edge of 'dValid') and that it must not remain low for more than 3 clocks (because data must trasnfer in max 4 clocks).*



LAB 5 : bus_protocol_property.sv

```
/*-----------------------------------------------------
      CHECK # 1. Check that once dValid goes high that it is consecutively
        asserted (high) for minimum 2 and maximum 4 clocks.
              Check also that once dValid is asserted (high) for 2 to 4 clocks that
              it does de-assert (low) the very next clock.
       -----------------------------------------------------*/
`ifdef check1
      property checkValid;
       @(posedge clk) disable iff (reset) $rose(dValid) |=> (dValid) [*2:4] ##1 $fell(dValid);
      endproperty
      assert property (checkValid) else $display($stime,,,"checkValid  FAIL");
`endif

      /*-----------------------------------------------------
        CHECK # 2. Check that data is not unknow and remains stable after dValid goes
                    high and until dAck goes high.
       -----------------------------------------------------*/
`ifdef check2
      property checkdataValid;
       @(posedge clk) disable iff (reset)
          $rose(dValid) |=> (!$isunknown(data) && $stable(data)) [*1:$] ##0 $rose(dAck);
endproperty
      assert property (checkdataValid) else $display($stime,,,"checkdataValid  FAIL");
`endif
```

LAB 5 : bus_protocol_property.sv

```
/*-----------------------------------------------------
      CHECK # 3. Check that 'dAck' and 'dValid' relationship is maintained to complete the
data transfer. In other words,

     'dack' going high signifies that target have accepted data and that master must de-
assert 'dValid' the clock after 'dack' goes high.

Note that since data must be valid for minimum 2 cycles, that 'dack' cannot go High
for at least 1 clock after the transfer starts (i.e. after the rising edge of 'dValid') and
that it must not remain low for more than 3 clocks (because data must trasnfer in max 4
clocks).
       -----------------------------------------------------*/
`ifdef check3
              property checkdAck;
               @(posedge clk) disable iff (reset)
                 $rose(dValid) |=> (dValid && !dAck) [*1:3] ##1 $rose (dAck) ##1 $fell (dValid);
              endproperty
              assert property (checkdAck) else $display($stime,,,"checkdAck  FAIL");
`endif
```

Fig. 18.8 LAB5: Data Transfer Bus Protocol: Answers

18.6 LAB6: Answers (Fig. 18.9)

LAB 6 : pci_protocol_property.sv

```
/*-----------------------------------------------------
     CHECK # 1. On falling edge of FRAME_, AD or C_BE_ cannot be unknown.
      -----------------------------------------------------*/
`ifdef check1
     property checkPCI_AD_CBE;
       @(posedge clk) disable iff (!reset_) $fell(FRAME_) |->
                                !($isunknown(AD) || $isunknown(C_BE_)) ;
     endproperty
     assert property (checkPCI_AD_CBE) else
$display($stime,,,"CHECK1:checkPCI_AD_CBE  FAIL\n");
`endif

     /*-----------------------------------------------------
     CHECK # 2. When IRDY_ and TRDY_ are asserted (low) AD or C_BE_ cannot be
unknown.
      -----------------------------------------------------*/
`ifdef check2
     property checkPCI_DataPhase;
       @(posedge clk) disable iff (!reset_) (!IRDY_ && !TRDY_) |->
                                !($isunknown(AD) || $isunknown(C_BE_)) ;
     endproperty
     assert property (checkPCI_DataPhase) else
$display($stime,,,"CHECK2:checkPCI_DataPhase  FAIL\n");
`endif

     /*-----------------------------------------------------
     CHECK # 3. FRAME_ can go High only if IRDY_ is asserted.
              In other words, master can signify end of cycle only if IRDY_ is
asserted.
      -----------------------------------------------------*/
`ifdef check3
     property checkPCI_Frame_Irdy;
       @(posedge clk) disable iff (!reset_) $rose(FRAME_) |-> !IRDY_;
     endproperty
     assert property (checkPCI_Frame_Irdy) else
$display($stime,,,"CHECK3:checkPCI_frmIrdy  FAIL\n");
`endif
```

Fig. 18.9 LAB6: PCI Protocol: Answers

LAB 6 : pci_protocol_property.sv

```
  /*-----------------------------------------------------
      CHECK # 4. TRDY_ can be asserted (low) only if DEVSEL_ is asserted (low)
       -----------------------------------------------------*/
`ifdef check4
      property checkPCI_trdyDevsel;
        @(posedge clk) disable iff (!reset_) !TRDY_ |-> !DEVSEL_;
      endproperty
      assert property (checkPCI_trdyDevsel) else
$display($stime,,,"CHECK4:checkPCI_trdyDevsel  FAIL\n");
`endif

      /*-----------------------------------------------------
      CHECK # 5. Once the cycle starts (i.e. at FRAME_ assertion)
                    C_BE_ should not float until FRAME_ is de-asserted
       -----------------------------------------------------*/
`ifdef check5
      property checkPCI_CBE_during_trx;
        @(posedge clk) disable iff (!reset_)
                $fell(FRAME_) |-> !($isunknown(C_BE_)) [*0:$] ##0 $rose(FRAME_);
      endproperty
      assert property (checkPCI_CBE_during_trx) else
$display($stime,,,"CHECK5:checkPCI_CBE_during_trx  FAIL\n");
`endif
```

Fig. 18.9 (continued)

Chapter 19
Functional Coverage

Ah, so you have done everything to check the design. But what have you done to check your test-bench? How do you know that your test-bench has indeed covered everything that needs to be covered? That's where Functional Coverage comes into picture. But first let us make sure we understand the difference between the good old Code Coverage and the new Functional Coverage methodology.

19.1 Difference Between Code Coverage and Functional Coverage

- Code Coverage
  - Derived directly from the design code; not user specified.
  - Evaluates to see if design structure has been covered (i.e., assign, branch, expression, state transition, etc.).
  - But does not evaluate the *intent* of the design

    if the user specified busGnt = busReq && (idle || !(reset));
    instead of the real *intent* busGnt = busReq && (idle **&&** !(reset));
    Code coverage won't catch it. For intent, you need both a robust test-bench to weed out functional bugs and a way to objectively predict how robust the test-bench is.
- Functional Coverage
  - User specified
  - Based on design specification (as we have already seen with 'cover' of an assertion)
  - Measures coverage of design intent
  - Control-oriented coverage.

    Have I exercised all possible protocols that read cycle supports (burst, non-burst, etc.)?

A. B. Mehta, *SystemVerilog Assertions and Functional Coverage*,
DOI: 10.1007/978-1-4614-7324-4_19,

– Data-oriented coverage

Have we accessed cache lines at all granularity levels (odd bytes, even bytes, word, quad-word, full cache line, etc.)?

– Other Examples

Did we issue transactions that access Byte followed by Qword followed by multiple Qwords (use SystemVerilog *transition* coverage).
Tag and Data Errors must be injected at the same time (use System-Verilog *cross* coverage).
A Write to L2 is followed by a Read from the same address (and vice versa). Again, the *transition* coverage will help you determine if you have exercised this condition.

19.2 Assertion Based Verification and Functional Coverage Based Methodology

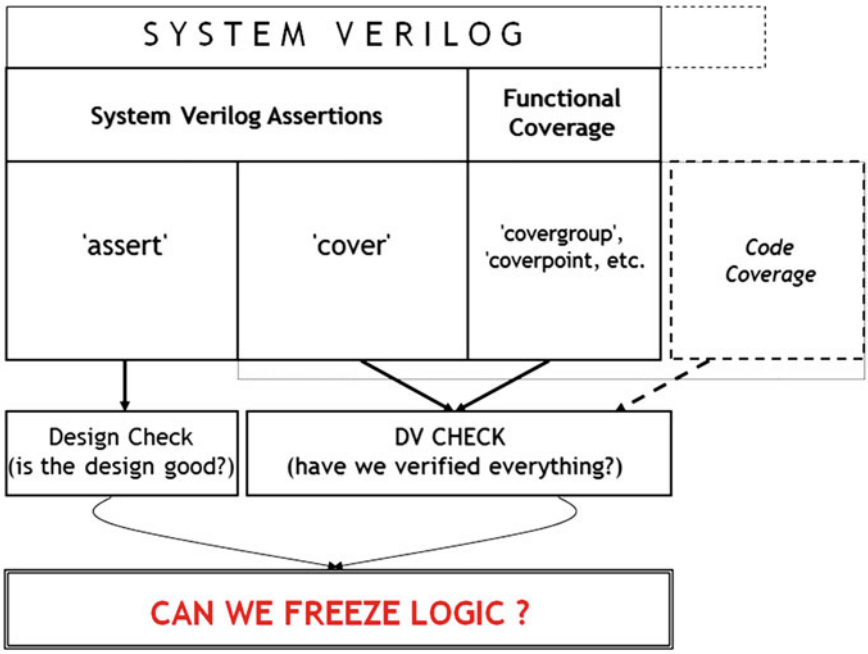


Fig. 19.1 Assertion based verification (ABV) and functional coverage (FC) based methodology

First let us examine the components of SystemVerilog language that contribute to Functional Coverage.

First component is the 'cover' statement associated with an assertion. This 'cover' statement allows us to measure temporal domain functional coverage. Recall that 'assert' checks for failures in your design and 'cover' sees if the property did get exercised (i.e. got covered). Pure combinatorial coverage is not sufficient. What I call 'low level' temporal domain conditions such as every req should be followed by a gnt. If this assertion does not fail, it could be because the logic is correct or *because you never really asserted* '*req*' *to start with*. 'cover' completes this story. We 'cover' exactly the same property that we 'assert'. In the req/gnt example, if 'cover' passes we know that the property did get exercised by the test-bench and it did not fail (if 'assert' did not fire).

Second component is the Functional Coverage language which is the gist of this entire section. Functional coverage allows you to specify the 'function' you want to cover via the so-called *coverpoints* and *covergroups*. More importantly, it also allows you to measure *transition* as well as *cross* coverage to see that we have indeed covered finer details of our design. This section will clarify all this.

Figure 19.1 clearly shows the different components of SystemVerilog as well as code coverage that all ties together to determine if a design have indeed been completely verified.

Here are some more points from project methodology point of view.

- Your test plan is (obviously) based on what functions you want to test (i.e. cover).
- So, create a Functional Cover Matrix based on your test plan that includes each of the functions (control and data) that you want to test.
  - Identify in this matrix all your functional covergroups/coverpoints (more on that coming soon).
  - Measure their coverage during verification/simulation process.
  - You may even automate updating the matrix directly from the coverage reports. That methodology is depicted in Fig. 19.2.
- Measure effectiveness of your tests from the coverage reports. To reiterate what we just discussed above since the following points are indeed the gist of what functional coverage allows you to accomplish.
  - For example, if your tests are accessing mostly 32 byte granules in your cache line, you will see byte, word, quadword coverage low or not covered. Change or add new tests to hit bytes/words, etc.
  - Or that the tests do not fire transactions that access Byte followed by Qword followed by multiple Qwords. Check this with *transition* coverage.
  - Or that Tag and Data Errors must be injected at the same time (*cross* coverage between Tag and Data Errors).
- 'cover' temporal domain assertions.
- And add more *coverpoints* for critical functional paths through design.

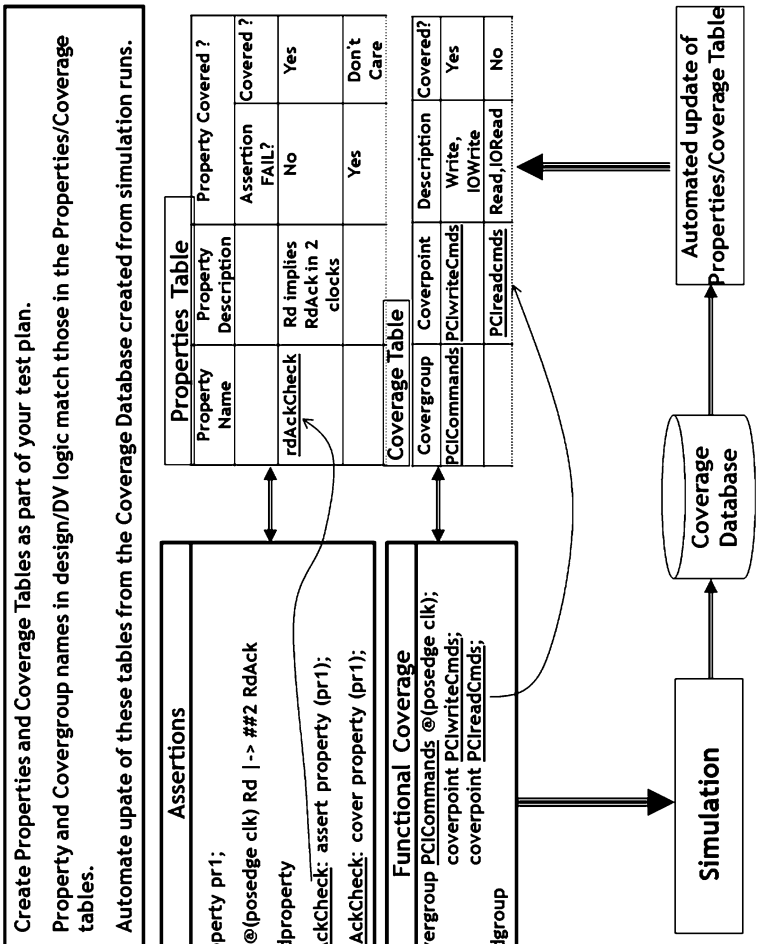


Fig. 19.2 Assertions and coverage closed loop verification methodology—I

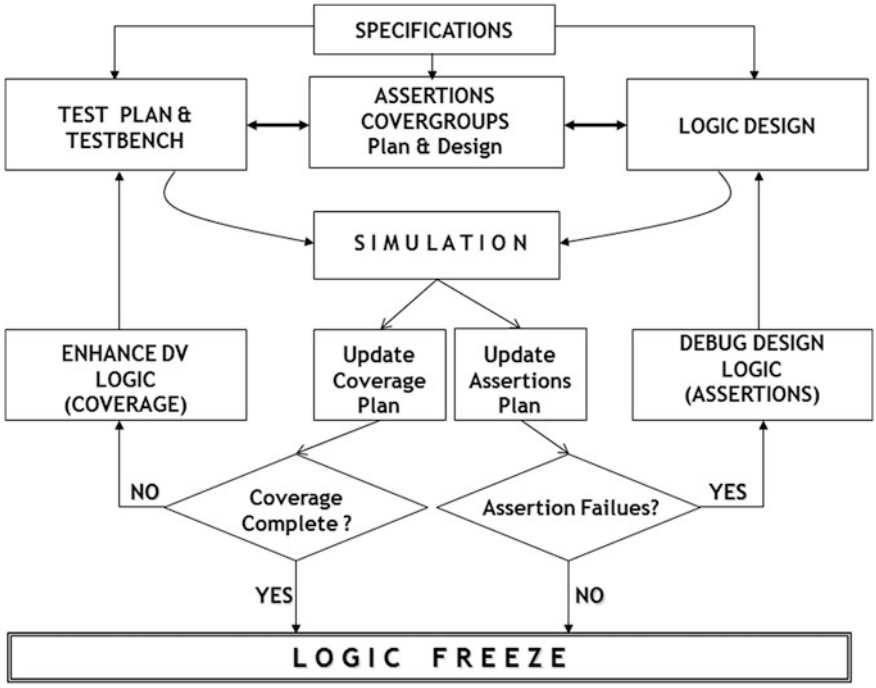


Fig. 19.3 Assertion and functional coverage closed loop verification methodology—II

  - For example, a Write to L2 is followed by a Read from the same address and that this happens from both processors in all possible write/read combinations.

- Remember to update your Functional Cover plan as verification progresses.
  - Just because you created a plan in the beginning of the project does *not* mean it's an end in itself.
  - As your knowledge of the design and it's corner cases increase, so should the exhaustiveness of your test plan and the functional cover plan.
  - Continue to add *coverpoints* for any function that you didn't think of at the onset.

Figures 19.2 and 19.3 show an assertion and coverage driven methodology.

1. For every 'assert' in a property, have an associated 'cover'. Give meaningful names to the property and assert Labels.
2. Create a Properties Table which automatically reads in your assertions and creates a FAIL/Covered matrix. If the assertion FAILs, well, fill in the FAIL column. If not and if gets covered, fill in the Covered column. How do we fill in this matrix? Read on…
3. Create a Functional Coverage plan with *covergroup* and *coverpoint*. Again give meaningful names to covergroup and coverpoint(s).

4. Create a Coverage Table that automatically derives the covergroup/coverpoint names from step 3 and creates a matrix for "Covered" results. This matrix is for those functions that are not covered by assertion 'cover' nor are they covered by code coverage. So, you need to carefully design your covergroups and coverpoints.
5. Simulate your design with assertions and functional cover groups.
6. Simulation will create a "coverage database". This database has all the information about failed assertions and 'cover'ed properties and covered covergroups and coverpoints.
7. Using EDA vendor provided API, shift through this database and update the Properties Table and Coverage Table.
8. Loop.

Advantage of such methodology is that you continuously know if you are spinning the wheel without increasing coverage. Without such continual measure you may keep simulating; bugs don't get reported; you start feeling comfortable only to realize later that the functional coverage was really inadequate. You were basically running the tests that target the same logic over and over again. If you have a methodology as described above you will have a correct notion of what functional logic to target to increase bug rate.

19.2.1 Follow the Bugs !!

- So, when do you *start* collecting coverage?
  - During initial stages of design both code and functional coverage will be low.
  - Code and Functional Coverage add to simulation overhead.
  - So, don't turn on code/functional coverage at the very 'beginning' of the project.
  - But what does 'beginning' of the project mean? When does the 'beginning' end?
- That's where the bugs come into picture!
  - Create Bug Report charts.
  - During the 'beginning' time, bug rate will (should) be high. All low hanging fruits are being picked ☺.
  - When the Bug Rate starts to drop; the 'beginning' has come to an 'end'.
  - That's when your existing test strategy is running out of steam ☺.
  - That's when you start code and functional coverage to determine.
- If new tests are simply exercising the same logic repeatedly.
- And which part of logic is not yet covered.
  - Develop tests for the uncovered functionality.
  - Your Bug Rate will again go up (guaranteed! ☺).

Chapter 20
Functional Coverage: Language Features

We will cover the following features in the upcoming sections.

1. covergroups and coverpoints for variables and expressions
2. automatic as well as user-defined coverage bins
3. 'bins' for transition coverage,
4. 'wildcard bins', 'illegal_bins', 'ignore_bins'
5. Cross Coverage
6. Coverage Options
7. Application: Coverage Methods and procedural activation of coverage methods.

20.1 Covergroup/Coverpoint

What is a covergroup?

I am taking the definition directly from the LRM since it is indeed well worded.

- 'covergroup' is a user defined type that allows you to collectively sample all those variables/transitions/cross that are sampled at the same clock (sampling) edge.
- "The 'covergroup' construct encapsulates the specification of a coverage model."
- A 'covergroup' can be defined in a 'package', 'module', a 'program', an 'interface' or a 'class'.

What is a coverpoint?

- A coverpoint is a variable or an expression that functionally covers design parameters (reg, logic, enum, etc.)
- Each coverpoint includes a set of bins associated with its sampled value or its value transition.

A. B. Mehta, *SystemVerilog Assertions and Functional Coverage*,
DOI: 10.1007/978-1-4614-7324-4_20,

- The so-called 'bins' can be defined by the user or created automatically by an EDA tool. A bin tells you the actual coverage measure.

OK, that's all fundamentals from the LRM. (the LRM authors did do a good job in writing some of this in English that hardware types can understand (like myself)..;-)).

Figure 20.1 makes it plenty simpler to explain covergroup and coverpoint.

20.2 SystemVerilog 'covergroup': Basics…

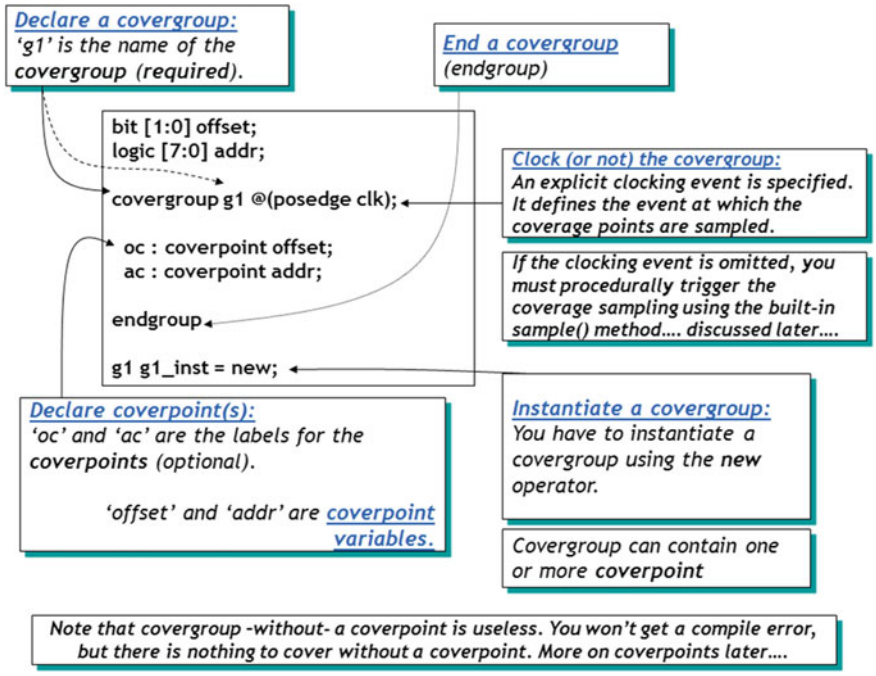


Fig. 20.1 'covergroup' and 'coverpoint'—basics

Figure 20.1 is self-explanatory with its annotations. Key syntax of the covergroup and coverpoint is pointed out. A few points to reiterate are as follows.

1. Covergroup without a coverpoint is useless *and* the compiler won't give an Error (at least the simulators that the author have tried).
2. Covergroup, as the name suggests, is a group of coverpoints, meaning you can have multiple coverpoints in a covergroup.
3. You have to instantiate the covergroup.

4. You may provide (not mandatory) a sampling edge to determine when the coverpoints in a covergroup get sampled. If the clocking event is omitted, you must procedurally trigger the coverage sample window using a built-in method called sample(). We will discuss sample() later in the chapter.
5. Not to reiterate a 'covergroup' can be declared in

   a. package
   b. interface
   c. module
   d. program
   e. class (we'll see an example soon).

Other points are annotated in Fig. 20.1. Carefully study them so that the rest of the chapter is easier to digest.

20.3 SystemVerilog coverpoint Basics…

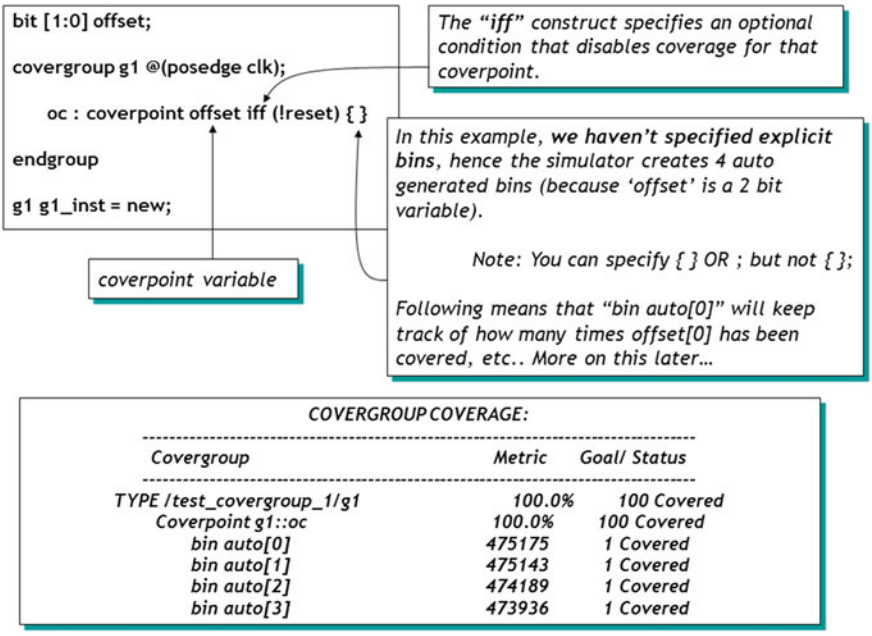


Fig. 20.2 'coverpoint'—basics

Coverpoint and bins associated with the coverpoint do all the work. The syntax for coverpoint is as shown in Fig. 20.2. 'covergroup g1' is sampled at (posedge clk). 'oc' is the coverpoint name (or label). This is the name by which simulation log refers to this coverpoint. 'oc' covers the 2-bit variable 'offset'.

We haven't yet covered 'bin's, so please hang on with this note here for a while. We will cover plenty of 'bin's in the upcoming sections. So, in this example, you do not see any 'bin' associated with the coverpoint 'oc' for variable 'offset'. Since there are no bins to hold coverage results, simulator will create those for you. In this example, the simulator will create 4 bins because 'offset' is a 2 bit variable. If 'offset' were a 3 bit vector, there would be 8 bins and so on. We will discuss a lot more on 'bin' in upcoming sections and hence I am showing only the so-called auto bins created by the simulator.

I haven't shown the entire test-bench but the simulation log (at the bottom of Fig. 20.2) shows that there are 4 auto generated bins called 'bin auto[0]'… 'bin auto[3]'. Each of these bins covers 1 value of 'offset'. For example, auto[0] bin covers 'offset = 0'. In other words, if 'offset==0' has been simulated, then auto[0] will be considered covered. Again, this will become clearer when we go through basics of 'bin's. Since all 4 bins of coverpoint 'oc' have been covered, the coverpoint 'oc' is considered 100 % covered, as shown in the simulation log. Now let us look at a real life example of covergroup/coverpoint.

20.3.1 Covergroup/Coverpoint Example …

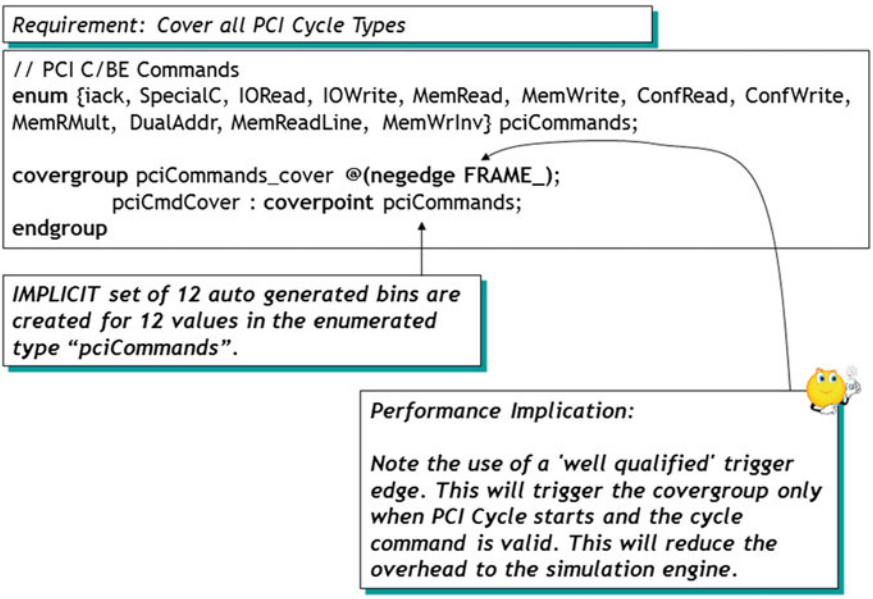


Fig. 20.3 'covergroup'/'coverpoint' example

PCI protocol consists of many different types of bus cycles. We want to make sure that we have covered each type of cycle. The enum type pciCommands (Fig. 20.3)

describes the cycle types. The covergroup specifies the *correct* sampling edge (that being negedge FRAME_) for the PCI Commands. In other words the sampling edge is quite important for performance reasons. If you sampled the same covergroup @ (posedge clk), there will be a lot of overhead because FRAME_ will fall only when a PCI cycle is to start. Sampling unnecessarily will indeed affect simulation performance.

In this example we have not specified any bins. So the simulator creates 12 auto bins for the 12 bus cycles types in the enum. Every time FRAME_ falls (sampled negedge) that the simulator will see if any of the cycle types in 'enum pciCommands' is simulated. Each of the 12 auto bin corresponds to each of the enum type. When a cycle type is exercised, the auto bin corresponding to that cycle (i.e. that 'enum') will be considered covered. Now, you may ask why code coverage won't cover this. Code coverage will indeed do the job. But I am building a small story around this example. We'll see how this covergroup will be then reused for transition coverage which *cannot* be covered by code coverage. Ok. now on to 'bin's.

20.4 SystemVerilog 'bins': Basics …

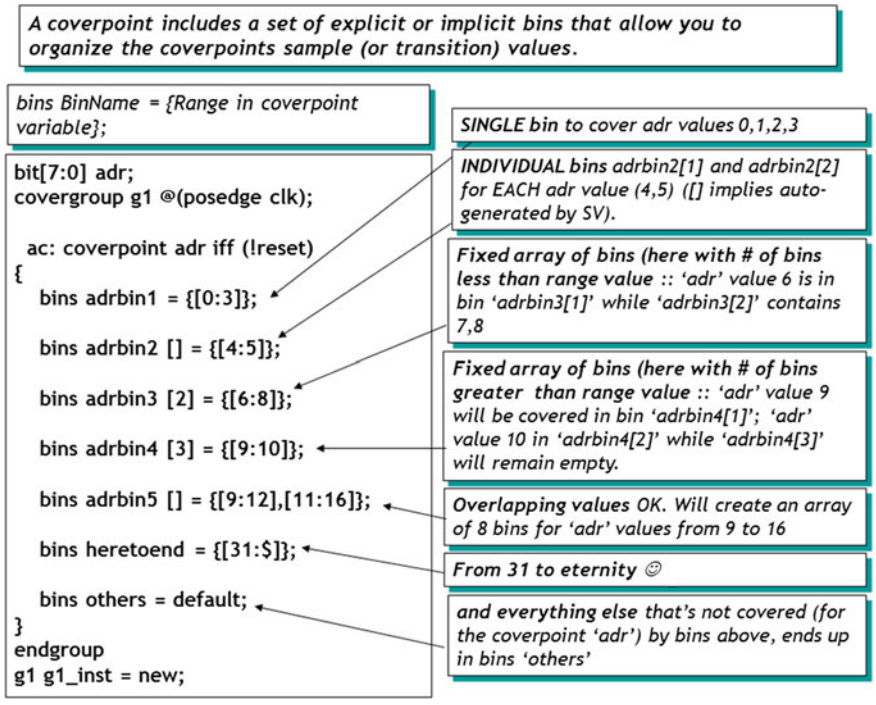


Fig. 20.4 'bins'—basics

What's a 'bin'? A 'bin' is something that collects coverage information (collect in a 'bin'). 'bin's are created for coverpoints. A coverpoint that is covering a variable (let's say the 8 bit 'adr' as shown in Fig. 20.4) and would like to have different values of that variable be collected in different collecting entities, the 'bin's will be those entities. A 'bin' allows you to organize the coverpoints sample (or transition) values.

You can declare bins many different ways for a coverpoint. Recall that bins collect coverage. From that point of view, you have to carefully choose the declaration of your bins.

OK, here's the most important point *very* easy to misunderstand. In the following statement, how many bins will be created? 16 or 4 or 1 and what will it cover?

bins adrbin1 = {[0:3]};

Answer : 1 bin to cover 'adr' values equal to '0' or '1' or '2' or '3'.

Note that 'bins adrbin1' is without the [] brackets. In other words, 'bins adrbin1' will *not* auto-create 4 bins for 'adr' values {[0:3]}, it will rather create only 1 bin to cover 'adr' values '0', '1', '2', '3'.

Very important point: Do not confuse {[0:3]} to mean that you are asking the bin to collect coverage for adr0 to adr15. {[0:3]} literally means 'adr' value =0, =1, =2, =3.

Another important point. What 'bins adrbin1 = {[0:3]}'; also says is that if we hit either of the 'adr' value ('0','1','2' or '3') that the single bin will be considered *completely* covered. Not very intuitive, I agree. But that's what the language semantics dictate. Again, you don't have to cover all four values to have "bins adrbin1" considered covered. You hit any one of those 4 values and the "adrbin1" will be considered 100 % covered.

But what if you want each value of the variable 'adr' be collected in separate bins so that you can indeed see if each value of 'adr' is covered explicitly. That's where 'bins adrbin2[] = {[4:5]};' comes into picture. Here '[]' tells the simulator to create two explicitly bins called adrbin2[1] and adrbin2[2] each covering the 2 'adr' values =4 and =5. adrbin2[1] will be considered covered if you exercised adr==4 and adrbin2[2] will be considered covered if adr==5 is exercised.

Other ways of creating bins are described in Fig. 20.4 with annotation to describe the nuances. Note that you can have 'less' or 'more' # of bins than the 'adr' values on the RHS of a bins assignment. How will 'bins' be allocated in such cases is explained in the figure. Note also the case {[31:$]} called 'bins heretoend'. What does '$' mean in this case? It means [32:255] since 'adr' is an eight bit variable.

Rest of the semantics is well described with annotation in the figure. Do study them carefully, since they will be very helpful when you start designing your strategy to create 'bins'.

20.4.1 Covergroup/Coverpoint with bins: Example …

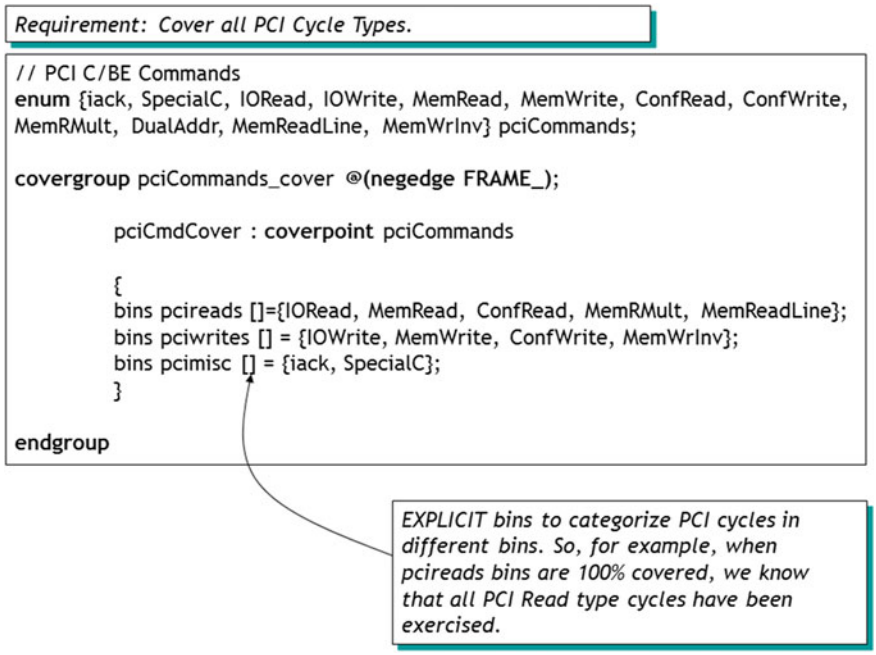


Fig. 20.5 'covergroup'/'coverpoint' example with 'bins'

Recall the example on PCI that we started in previous section. It's story continues here.

In Fig. 20.5 we are assigning different groups of PCI commands to different bins.

Recall that [] means auto generated bins. Hence, for example, since 'bins pcireads[]' in Fig. 20.5 has 5 variables (enum type in this example), 5 bins will be created—one for each enum type. This way of creating bins is very useful because in the complex maze of features to cover, it is sure nice to have a clear distinction among different functional groups. Here pcireads[] (5 bins) covers all PCI Read Cycles; pciwrites[] (4 bins) covers all PCI Write Cycles and for the special cycles, there is the pcimisc[] (2 bins).

20.4.2 SystemVerilog 'covergroup': Formal and Actual Arguments

Figure 20.6 outlines the following points.

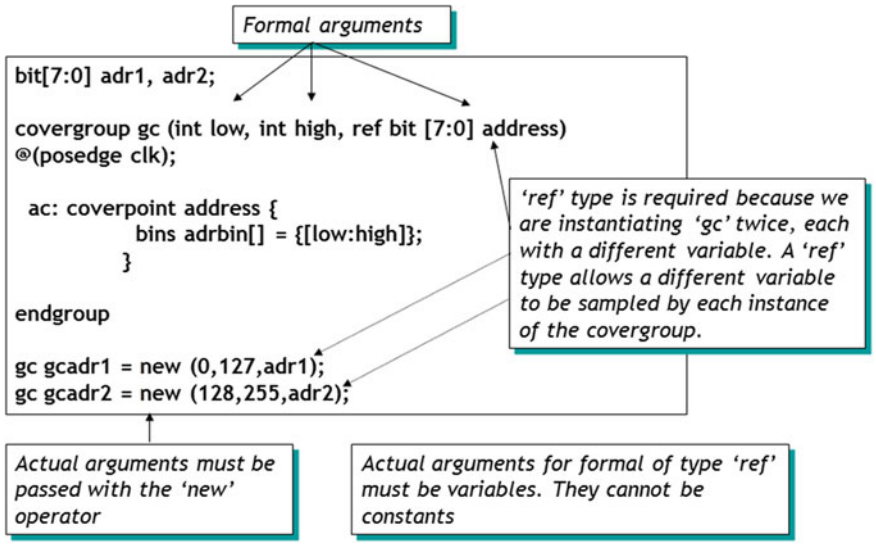


Fig. 20.6 'covergroup'—formal and actual arguments

1. Covergroup can be parameterized for reuse
2. You have to use 'ref' type since covergroup 'gc' has been instantiated twice. 'Ref' type is required when you pass variables as actual to a formal. In other words, if you were passing a constant you would *not* need a 'Ref' type as shown in Fig. 20.6.
3. Actual arguments are passed when you instantiate a covergroup.
4. This is an example of reusability. Instead of creating two covergroups; 1 for 'adr1' and another for 'adr2', we have created only 1 covergroup called 'gc' which has a formal called 'address'. We pass 'adr1' to 'address' in the instance gcadr1 and pass 'adr2' to 'address' I n the instance gcadr2. We also pass the range of adr1 and adr2 to be covered with each instance. In short, it is a good idea to create parameterizable covergroups, as the situation permits. They can be useful not only within a project but also across projects.

Exercise: How many bins will be created for 'bins adrbin[]' for each instance ('gcadr1' and 'gcadr2') of covergroup 'gc'?

20.4.3 'covergroup' in a 'class'

So where do you use or declare this 'covergroup'? One of the best places to embed a coverage group is within a 'class'. Why a class? Here are some reasons. (Note—discussion of 'class' is beyond the scope of this book. The author is assuming familiarity with SystemVerilog 'class').

```
class xyz;
  bit [3:0] m_x;
  int m_y;
  bit m_z;

  covergroup xyzCover @(m_z);
            coverpoint m_x;
            coverpoint m_y;
  endgroup

  function new();
     xyzCover xyzCovInst = new;
  endfunction
endclass
```

- *By embedding a 'covergroup' within a class definition, the 'covergroup' provides a simple way to cover as part of class definition the class properties (modular development)*
- *A 'class' can have more than one 'covergroup'*

Fig. 20.7 'covergroup' in a SystemVerilog class (courtesy LRM 1800-2005)

- An embedded covergroup defines a coverage model for protected and local properties.
- Class members can be used in coverpoint expressions, coverage constructs, option initialization (we'll see option initialization in Chap. 22), etc.
- By embedding a coverage group within a class definition, the covergroup provides a simple way to cover a subset of the class properties.
- This style of declaring covergroups allow for modular verification environment development.

OK, let us see what Fig. 20.7 depicts.

'covergroup xyzCover' is sampled on any change on variable 'm_z'. This covergroup contains two coverpoints, namely 'm_x' and 'm_y'. Note that there are no explicit bins specified for the coverpoints. How many bins for each coverpoint will be created? As an exercise, please refer to previous sections to figure out.

Note that covergroup is instantiated within the 'class'. That makes sense since the covergroup is embedded within the class. Obviously, if you do not instantiate a covergroup in the 'class', it will not be created and there will not be any sampling of data.

Finally, a 'class' can indeed have more than one 'covergroup' as shown Fig. 20.8.

```
class xyz;
  bit [3:0] m_x;
  int m_y;
  bit m_z, m_a;

  covergroup  m_xCover @(m_z) coverpoint m_x;
   covergroup  m_yCover @(m_a) coverpoint m_y;

  endgroup

  function new();
     m_xCover m_x_CovInst = new;
  endfunction

 function new();
     m_yCover m_y_CovInst = new;
  endfunction
endclass
```

Fig. 20.8 Multiple 'covergroup' in a SystemVerilog class

20.5 'cross' Coverage

'cross' is a very important feature of functional coverage. This is where code coverage completely fails. Figure 20.9 describes the syntax and semantics.

Two variables 'offset' and 'adr' are declared. Coverpoint for 'offset' creates four bins called ofsbin[0]… ofsbin[3] for the four values of 'offset' namely, 0, 1, 2, 3. Coverpoint 'adr' also follows the same logic and creates adrbin[0]…adrbin[3] for the four values of 'adr' namely, 0, 1, 2, 3.

adr_ofst is the label given to the 'cross' of ar, ofst. First of all, the 'cross' of 'ar' (label for coverpoint adr) and 'ofst' (label for coverpoint offset) will create another set of 16 bins (four bins of 'adr' * four bins of 'offset'). These 'cross' bins will keep track of the result of 'cross'. However, what does 'cross' mean?

Four values of 'adr' need to be covered. 0, 1, 2, 3. Let us assume adr==2 has been covered (i.e. adrbin[2] is covered). Similarly, there are four values of 'offset' that need to be covered (0, 1, 2, 3) and that offset==0 has also been covered (i.e. ofsbin[0] has been covered). However, have we covered 'cross' of adr=2 (adrbin[2])and offset=0 (ofsbin[0])? Not necessarily. 'cross' means that adr=2 and offset=0 must be true 'together' at some point in time. This does *not* mean that they need to be 'covered' at the *same* time. It simply means that (e.g.) if adr=2 that it should remain at that value until offset=0. This will make both of them true 'together'. If that is the case, then the 'cross' of adrbin[2] and ofsbin[0] will be considered 'covered'.

In the simulation log in Fig. 20.10, we see that both adrbin[2] and ofsbin[0] have been individually covered 100 %. However, their 'cross' has not been covered.

Let us look at the simulation log further.

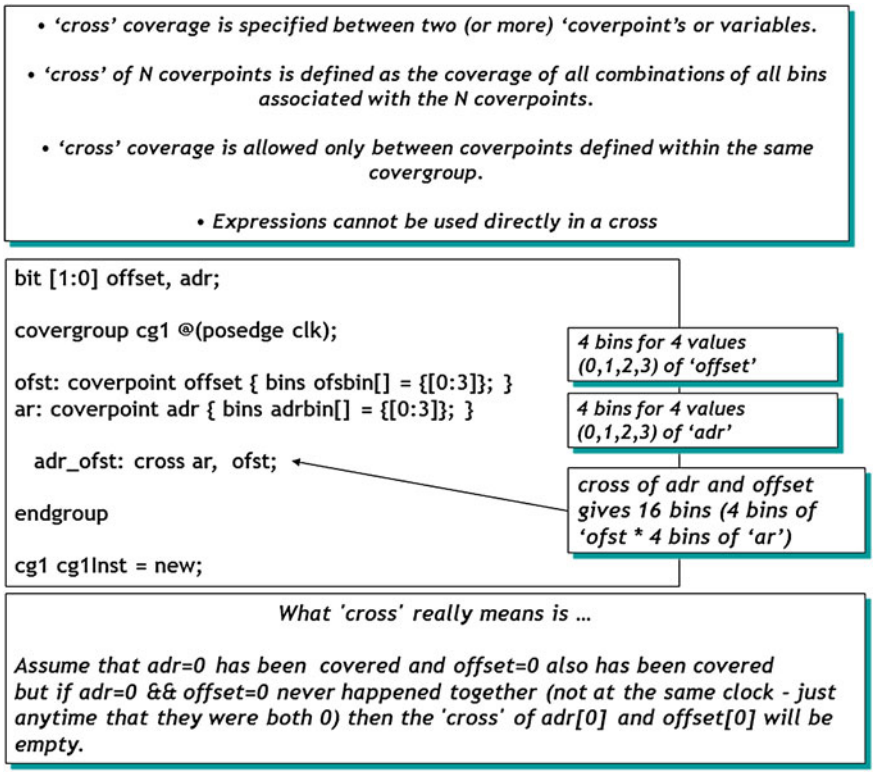


Fig. 20.9 'cross' coverage—basics

First, you will see the 4 bins (ofsbin[0] to ofsbin[3]) of coverpoint cg1::ofst. All 4 bins are covered and hence coverpoint cg1::ofst is 100 % covered. Next, you will see the 4 bins (adrbin[0] to adrbin[3]) of coverpoint cg1::ar. All bins are covered here as well and so is the coverpoint cg1::ar.

Now let us look at the 'cross' of 4bins*4bins=16 bins coverage. Both 'ofst' and 'ar' are 100 % covered—but- following 3 cases (among many others) are not covered because whatever values the test-bench drove, these bins never had the same value at any given point in time (e.g., adrbin[2] is '2' at time t, then ofsbin[0] should be '0' either at time t or any time after that as long as adrbin[2] = '2').

Hence,

bin <adrbin[2],ofsbin[0]> 0 1 ZERO

Similarly, there are other cases of 'cross' that are not covered as shown in the simulation log. Such a log will clearly identify the need to enhance your test-bench. To reiterate, such 'cross' cannot be derived from code coverage.

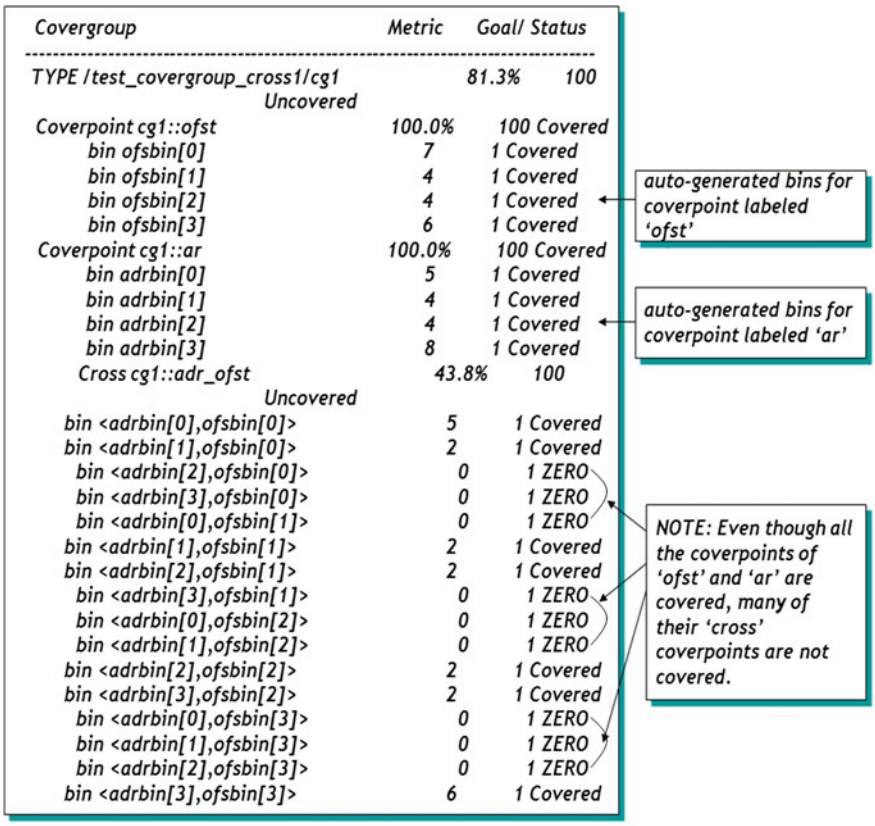


Fig. 20.10 'cross' coverage—simulation log

Let us look at further nuances of 'cross' as shown in Fig. 20.11.

Figure 20.11 shows how cross is achieved between an enum type and a bit type. Idea is to show how cross coverpoint/bins are calculated. The figure describes different ways 'cross' bins are calculated.

Recall that a 'cross' can be defined only between two coverpoints, meaning you must have an explicit coverpoint for a variable in order to cross with another coverpoint. That is where there is an anomaly when it comes to enum type. The enum type 'color' has no coverpoint defined for it. Yet, we are able to use it in 'cross'. That is because the language semantics implicitly creates a coverpoint for the enum type 'color' and track it's cross coverage. Other than an enum type, you must create a coverpoint of a variable in the covergroup, if you need to 'cross' it with another variable coverpoint. Note also that you use the 'label' of each coverpoint in the 'cross' statement, *not* the name of the variable. Again, the exception here is the enum type for which we use the enum type name, as in 'color' (because we didn't have to create a coverpoint for it—so there is no coverpoint name).

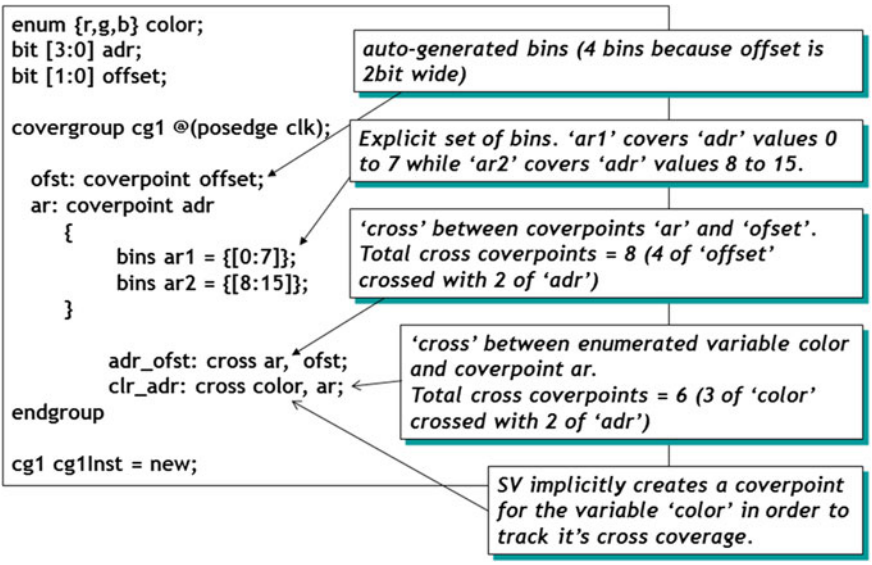


Fig. 20.11 'cross'—example (further nuances)

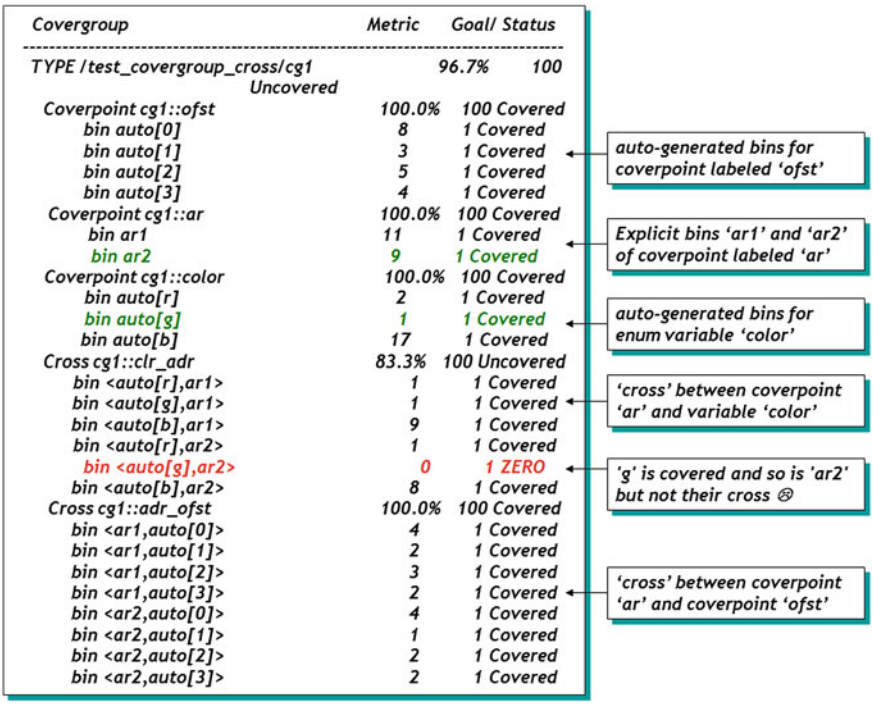


Fig. 20.12 'cross' example—simulation log

Please study this and other figures carefully since they will act as guideline for your projects. A simulation log of this example is presented in Fig. 20.12. The annotations describe what's going on.

20.6 More 'bins'

20.6.1 'bins' for Transition Coverage

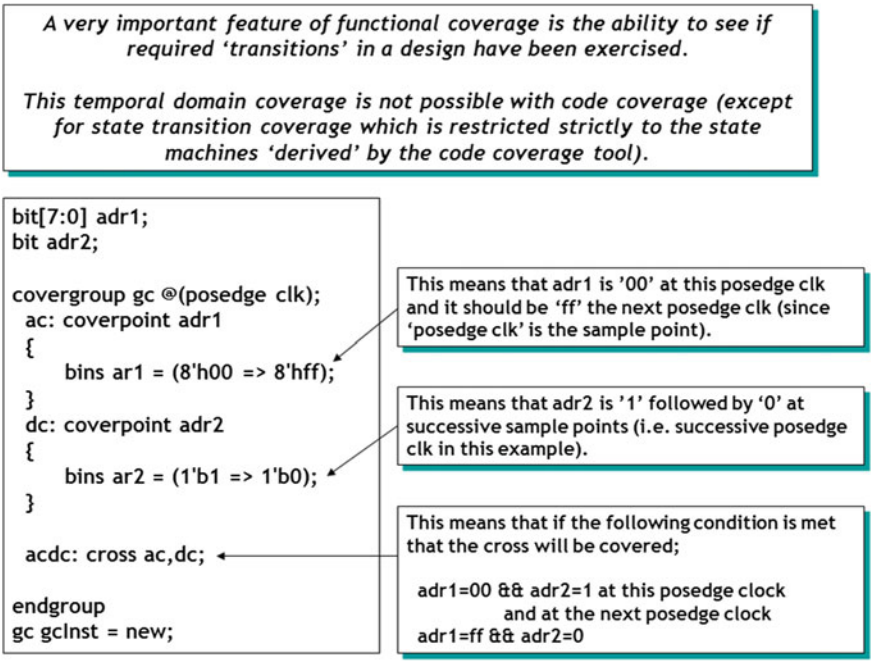


Fig. 20.13 'bins' for transition coverage

As noted in Fig. 20.13, this is by far the most useful feature of functional coverage. Transaction level transitions are very important to cover. For example, did CPU issue a read followed by write-invalid? Did you issue a D$miss followed by a D$hit cycle? Such transitions are where the bugs occur and we want to make sure that we have indeed exercised such transitions.

Figure 20.13 explains how the semantics work. Note that we are addressing both the 'transition' as well as the 'cross' of 'transition' coverage.

There are two transitions in the example.

Bins ar1 = (8′h00 => 8′hff); which means that adr1 should transition from '0' to 'ff' on two consecutive posedge of clk. In other words, the test-bench must exercise this condition for it to be covered.

Similarly, there is the 'bins ar2' that specifies the transition for adr2 (1 => 0).

The cross of transitions is shown at the bottom of the figure. Very interesting how this works. Take the first values of each transition (namely, adr1=0 and adr2=1). This will be the start points of cross transition at the posedge clk. If at the next (posedge clk) values are adr1='ff' and adr2=0, the cross transition is covered.

More on the 'bins' of transition is shown in the Fig. 20.14. In the figure, different styles of transitions have been shown. 'bins adrb2' requires that 'adr1' should transition from 1=>2=>3 on successive posedge clk. Of course, this transition sequence can be of arbitrary length. 'bins adrb3[]' shows another way to specify multiple transitions. The annotation in the figure explains how we get 4 transitions.

'bins adrb5' is (in some sense) analogous to the consecutive operator of assertions. Here 'hf [*3] means that adr1='hf should repeat 3 times at successive posedge clk.

Similarly, the non-consecutive transition ('ha [->3]) means that adr1 should be equal to 'ha, 3 times and not necessarily at consecutive posedge clk. Note that just as in non-consecutive operator, here also 'ha need to come 3 times with arbitrary number of clocks in-between their arrival and that 'adr1' should *not* have any other value in-between these three transitions. The simulation log shows the result of a test-bench that exercises all the transition conditions.

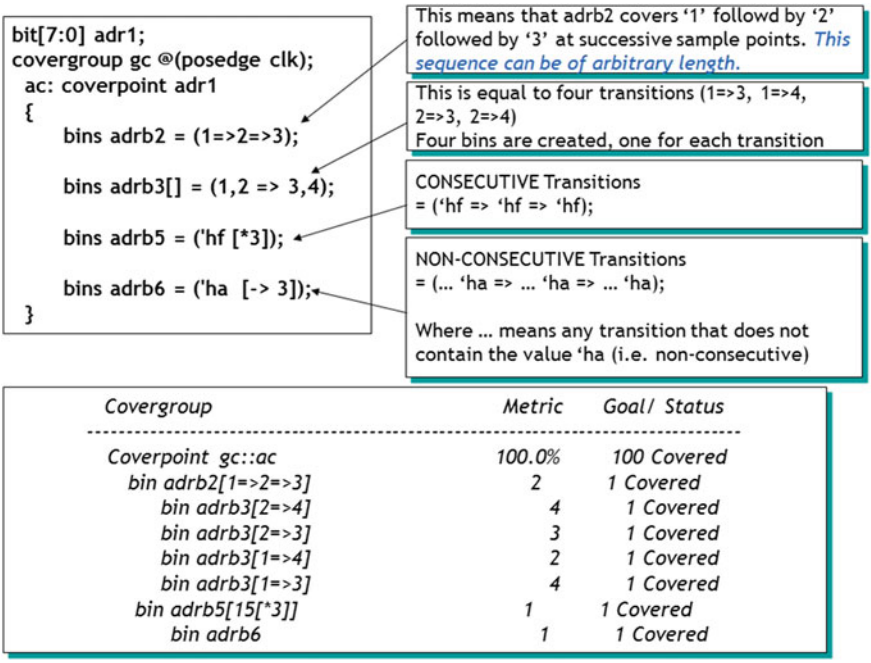


Fig. 20.14 'bins'—transition coverage further features

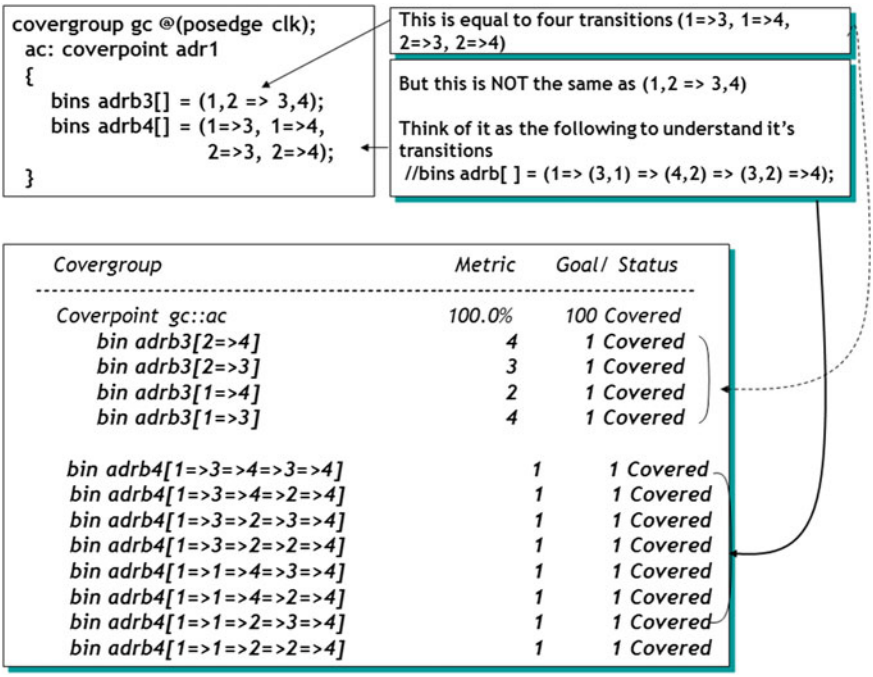


Fig. 20.15 'bins' for transition—example with simulation log

One more example of transition coverage in Fig. 20.15.

This figure shows a very interesting semantic feature of transition. Note that 'bins adrb3[] = (1, 2 => 3, 4)' is *not* the same as 'bins adrb4[] = (1=>3, 1=>4, 2=>3, 2=>4)'. What? Didn't we just say they were equivalent. Well, not really.

'bins adrb3[] = (1, 2 => 3, 4)' means transitions ***(1=>3, 1=>4, 2=>3, 2=>4)***. BUT

'bins adrb4[]=(1=>3, 1=>4, 2=>3, 2=>4)' means

[1=>3=>4=>3=>4]
[1=>3=>4=>2=>4]
[1=>3=>2=>3=>4]
[1=>3=>2=>2=>4]
[1=>1=>4=>3=>4]
[1=>1=>4=>3=>4]
[1=>1=>2=>3=>4]
[1=>1=>2=>2=>4]

Is that intuitive? I don't think so. However, the following will explain.

'bins adrb4[]=(1=>3, 1=>4, 2=>3, 2=>4)' is *equivalent* to

'bins adrb4[]=(1=>(3, 1)=>(4, 2)=>(3, 2)=>4)'

If you see the equivalent definition, you will be able to understand the transition. Study them carefully, you will figure out why the transitions look the way they do.

In short, you need to be careful how you specify transition coverpoints.

Now let us turn back to our favorite PCI example that we have been following. We started with simple coverage, moved to 'bins' coverage and now we will see the 'transition' coverage. This is the reason we were building on the same example showing how such a coverage model can be written starting with a simple model.

Figure 20.16 shows the same enum type and same bins. But in addition, it now defines two transition bins named R2 W (for Read to Write) and W2R (for Write to Read).

Bins R2 W means that all possible Read cycles types are followed by all possible Write cycles. In this example that means we must cover the following transactions

- IORead => IOWrite; IORead => MemWrite; IORead => ConfWrite;
- MemRead => IOWrite; MemRead =>MemWrite; MemRead => ConfWrite;
- ConfRead => IOWrite; ConfRead => MemWrite; ConfRead => ConfWrite;
- MemReadLine => IOWrite; MemReadLine => MemWrite; MemReadLine => ConfWrite;

Same type of transitions for bins W2R[].

Requirement: Cover all PCI Cycle Types and transitions among Read and Write cycles.

```
// PCI C/BE Commands
enum {iack, SpecialC, IORead, IOWrite, MemRead, MemWrite, ConfRead, ConfWrite,
      MemRMult, DualAddr, MemReadLine, MemWrInv} pciCommands;

covergroup pciCommands_cover @(negedge FRAME_);

          pciCmdCover : coverpoint pciCommands

          {
          bins pcireads [] = {IORead, MemRead, ConfRead, MemRMult, MemReadLine};
          bins pciwrites [] = {IOWrite, MemWrite, ConfWrite, MemWrInv};
          bins pcimisc [] = {iack, SpecialC};

          bins R2W [] = (IORead, MemRead,ConfRead, MemReadLine => IOWrite,
                         MemWrite, ConfWrite);
          bins W2R [] = (IOWrite, MemWrite,ConfWrite => IORead, MemRead,
                         ConfRead, MemReadLine);
          }
endgroup
```

Fig. 20.16 Example of PCI Cycles transition coverage

As you notice, this is quite powerful. Many bugs occur when there is a transition from transaction type to the next. You have to make sure that your testbench indeed covers such transitions.

20.6.2 'wildcard' 'bins'

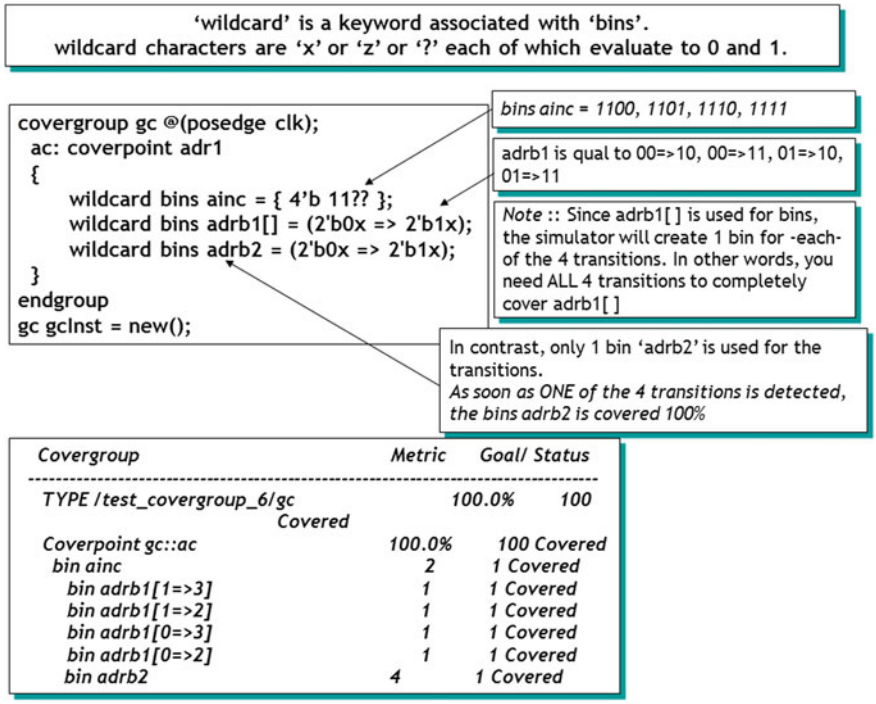


Fig. 20.17 Wildcard 'bins'

Since no one likes to type a sequence repeatedly, we create don't care (or as the functional coverage lingo calls it 'wildcard' bins). Self-explanatory. As shown in Fig. 20.17, you can use either an 'x' or a 'z' or '?' (doesn't this look familiar to Verilog?) to declare wildcard bins. Note that such bins must precede with the keyword 'wildcard'. 'wildcard bins ainc' specifies that adr1 values 1100, 1101, 1110, 1111 need to be covered.

Note also 'wildcard bins adrb1[]' and 'wildcard bins adrb2'. One creates implicit ([]) 4 bins while the other creates only 1 bin. The one that creates 4 explicit bins will check to see that—*all*—4 t transitions take place. While adrb2 that creates only 1 bin will be considered covered if—*any*—of the 4 transitions take place.

20.6.3 'ignore_bins'

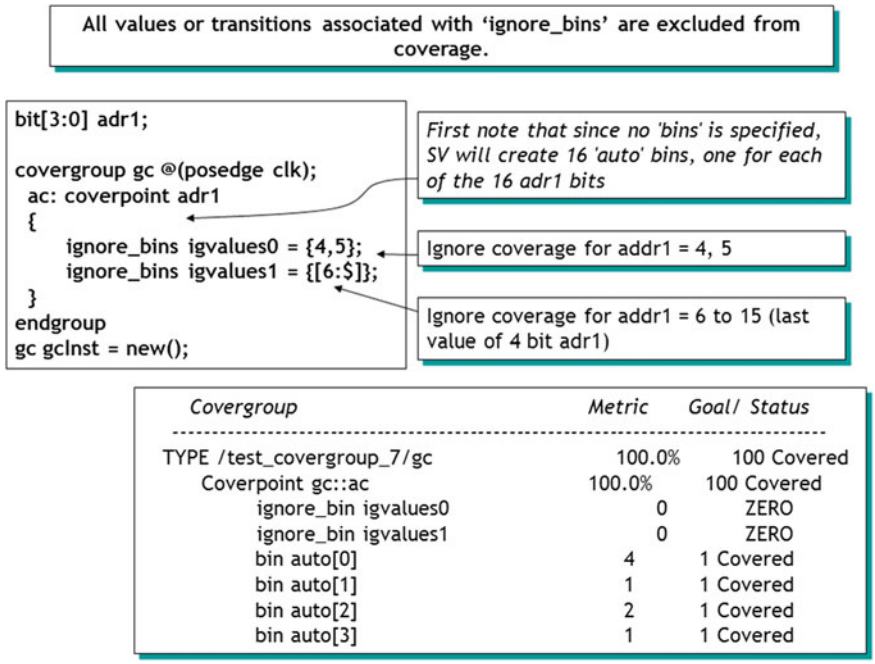


Fig. 20.18 'ignore_bins'—Basics

'ignore_bins' is very useful when you have a large set of bins to be defined. Instead of defining every one of those, if you can identify the ones that are not of interest, then you can simply define 'ignore_bins'. The ones that are specified to be ignored, will indeed be ignored and rest will be covered.

As we noted at the onset of this chapter, when there is no explicit 'bins' defined for a coverpoint, the simulator creates all possible bins that the 'covered' variable requires. In Fig. 20.18, only 'ignore_bins' are specified in the coverpoint adr1 but no 'bins'. This means that the simulator will first create all 16 bins (adr1 is 4 bit wide) for adr1. Then it will ignore value 4, 5 and 6, 7, 8, 9, 10, 11, 12, 13, 14, 15 and cover only adr1=0,1,2,3. This is reflected in the simulation log at the bottom of Fig. 20.18.

20.6.4 'illegal_bins'

'illegal_bins' is interesting in that it will complain, if you *do* cover a given scenario. In Fig. 20.19, we refer to the same old 'adr1'. 16 auto bins are created for

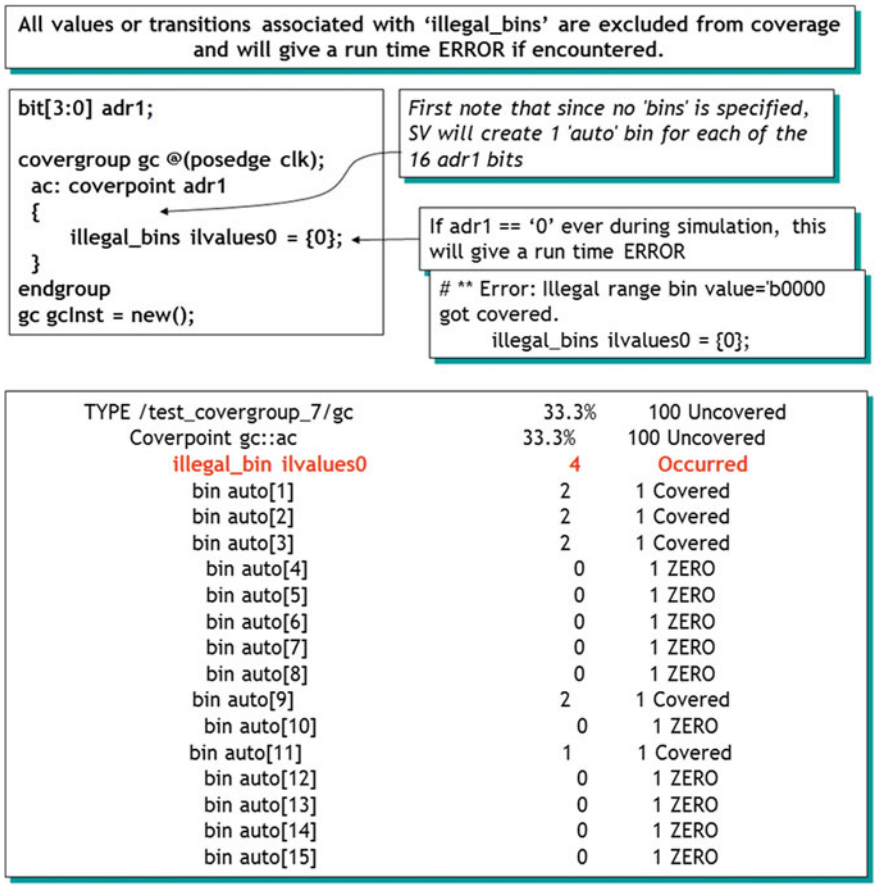


Fig. 20.19 'illegal_bins'

coverpoint 'adr1' since we don't explicitly declare any bins for it. And we say that if the test-bench ever hits adr1==0, that it should be considered illegal. Coverage of adr1==0 should not occur. As seen from the simulation log, coverage of adr1=0 results in an Error.

20.6.5 'binsof' and 'intersect'

Ok, now we are in some seriously esoteric territory! Fig. 20.20 shows that 'coverpoint b' has two bins; one is called 'bb' and has value from 0 to 12 of 'b'. bins cc on the other hand has values 13,14,15,16 of 'b' that need to be covered. So far so good. Then we declare a 'cross' of a, bc. So, let us first see what this cross looks like.

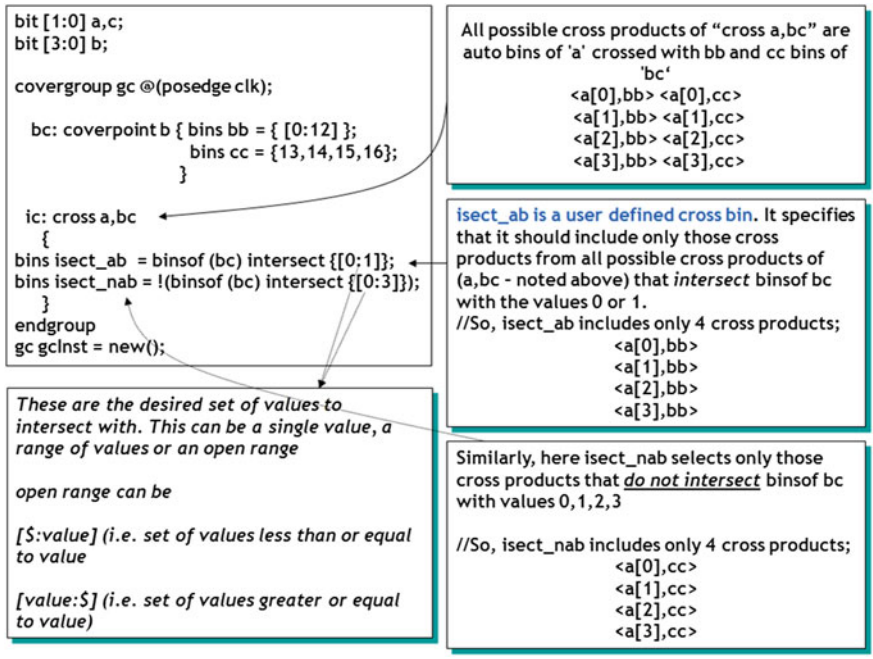


Fig. 20.20 'binsof' and 'intersect'

'a' has 4 implicit bins a[0], a[1], a[2], a[3] for four values 0,1,2,3 and 'bc' has two bins 'bb' and 'cc. So the 'cross a,bc' produces

<a[0],bb> <a[0],cc>
<a[1],bb> <a[1],cc>
<a[2],bb> <a[2],cc>
<a[3],bb> <a[3],cc>

We are moving along just fine—right? But now it gets interesting. We don't want to cover all 'cross' bins into our 'cross' of 'a' and 'bc'. We want to 'intersect' them and derive a new subset of the total 'cross' set of bins.

bins isect_ab = binsof (bc) intersect {[0:1]};

says that take all the bins of 'bc' (which are 'bb' and 'cc') and intersect them with the 'values' 0 and 1. Now note carefully that 'bb' carries values {[0:12]} which includes the values 0 and 1, while 'cc' does not cover 0 or 1. Hence, only those cross products of 'bc' that cover 'bb' are included in this intersect. Note that the below mentioned subset is selected from the 'cross' product shown above.

<a[0],bb>, **<a[1],bb>**, **<a[2],bb> <a[3],bb>**

Now onto the next intersect.

bins isect_nab = ! (binsof (bc) intersect {[0:3]})

Similarly, first, note that here we are using negation of binsof. So this'bins' statement says, take the intersect of binsof (bc) and {[0:3]} and discard them from the 'cross' of a, bc. Keep only those that do not intersect. Note that {[0:3]} again fall into the bins 'bb' and would have resulted in exactly the same set that we saw for the non-negated intersect. Since this one is negated it will ignore cross with 'bb' and only pick the 'bins cc' from the original 'cross' of a, bc.

<a[0],cc>, <a[1],cc>, <a[2],cc>, <a[3],cc>

Chapter 21
Performance Implications of Coverage Methodology

21.1 Know *what* you Should Cover

- Don't cover the entire 32-bit address bus.
  - Cover only the addresses of interest (e.g., Byte/word/dword aligned; start/end address; bank crossing address, etc.)
- Don't cover the entire counter range
  - Cover only the rollover counter values (transition from all 1′s to all 0′s)
- No need to cover the entire 2 K Fifo
  - Cover only fifo full, fifo empty, fifo full crossed with fifo_push, fifo empty crossed with fifo read, etc.
- Auto generated bins are both a convenience and a nuisance. They may create a lot of clutter with auto-generated bins that may not be relevant. Be judicious in usage of auto generated 'bins'
- Use 'cross' and 'intersect' to weed out unwanted 'bins'.

21.2 Know *when* you Should Cover

- Enable your cover points only when they are meaningful
  - Disable coverage during 'reset'
  - Cover 'test mode' signals only when in test mode (for example, JTAG TAP Controller TMS asserted)
  - Make effective use of coverage methods such as 'start', 'stop', 'sample' (more on this later…)
  - Do not repeat with covergroups what you have covered with SVA 'cover'

A. B. Mehta, *SystemVerilog Assertions and Functional Coverage*,
DOI: 10.1007/978-1-4614-7324-4_21,

– Make effective use of covergroup 'trigger' condition
– Make effective use of the 'action' block associated with 'cover' to activate a covergroup.

If some of these points (e.g. 'trigger') don't quite make sense, please hold on. We will be covering such features in upcoming sections.

21.3 When to 'Cover' (Performance Implication)

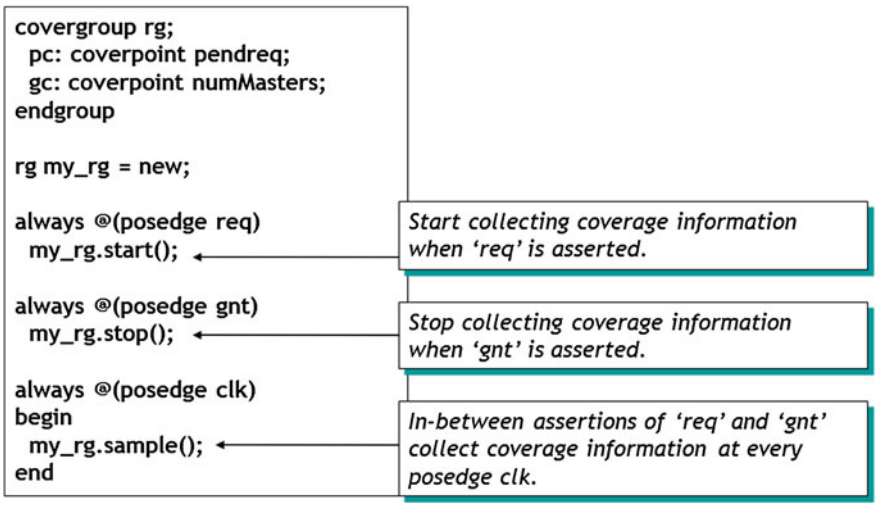


Fig. 21.1 Functional coverage—performance implication

Functional coverage should be carefully collected as discussed above. The language does allow tasks that allow you to control when to start collecting coverage and when to stop. These tasks can be associated with an instance of a covergroup and invoked from procedural block.

Figure 21.1 shows the covergroup 'rg' with two coverpoints 'pc' and 'gc'. 'pc' covers all the pending requests and 'gc' covers the number of masters on the bus when those requests are made. 'my_rg' is the instance of this covergroup.

Since we want to start collecting pending requests at the assertion of req. When the requests are granted, we don't want to cover pending requests and number of masters any more. 'gnt' related cover can be another covergroup.

Simple control but very good performance improvement. Use it wisely to speed up your simulation and a more meaningful coverage log.

Lastly, there is the sampling edge task sample() which derives its sampling edge from "always @ (posedge clk)" and applies it to 'my_rg' as its sampling edge. This also tells us that we can have covergroup specific sampling edges. Very good

feature. Note that my_rg.sample() will 'start' when my_rg.start() is executed and will stop when my_rg.stop() is executed. This is about as easy as it gets when it comes to controlling collection of coverage information.

21.4 Application: Have you Transmitted All Different Lengths of a Frame?

This application exemplifies the use of
- *local variables*
- *subroutine call associated with an expression to update a variable*
- *covergroup triggered from an explicit event.*

```
logic [7:0] FrameLngth = 0;
event measureFrameLength;

covergroup length_cg @(measureFrameLength );
        coverpoint FrameLngth;
endgroup

task store_Frame_Lngth;
input [7:0] x;
        FrameLngth = x;
        -> measureFrameLength;
endtask

sequence frmLength;
int cnt;
        (TX_EN, cnt=1)  ##1  ((TX_EN, cnt++)[*0:$])
        ##1 (!TX_EN, store_Frame_Lngth(cnt))
endsequence

property frameLength;
        @(posedge TX_CLK) $rose(TX_EN) |-> frmLength;
endproperty

fLength: assert property (frameLength);
```

Fig. 21.2 Application—Have you transmitted all different lengths of a frame?

This good application combines local variables, subroutine calls, covergroups and interaction with procedural code outside of the assertion. Here's how it works (Fig. 21.2).

Read this example bottom up.

Property frameLength says that when the rising edge of TX_EN is sampled that we should check the length of the transmitted frame using sequence frmLength.

Sequence frmLength declares a local variable ‘cnt’ and at TX_EN==1, initializes cnt=1. One clock later (##1) it increments cnt forever ((TX_EN,cnt ++)[*0:$]) until TX_EN deasserts (falls). At that time, we call a task (i.e. a subroutine) called store_Frame_Lngth(cnt) and provide it the final count as a parameter. This final count is the length of the Frame that started with TX_EN assertion.

The task store_Frame_Lngth takes the ‘cnt’ as input and assigns it to ‘logic’ type FrameLngth and triggers a named event called measureFrameLength.

Now the covergroup length_cg triggers at ‘measureFrameLength’ edge, which we just triggered explicitly from task store_Frame_Lngth. The coverpoint covers FrameLngth.

In short, we measure the Frame Length starting assertion of TX_EN until deassertion of it. We measure the frame length between assertion and deassertion of TX_EN and cover it. With every new assertion of TX_EN, we measure the length of a new frame.

Note that “coverpoint FrameLngth” does not specify any explicit bins. That will create 256 explicit bins each containing a frame length. This way we make sure that we have covered all (i.e. 256) different frame lengths.

Chapter 22
Coverage Options (Reference Material)

A. B. Mehta, *SystemVerilog Assertions and Functional Coverage*,
DOI: 10.1007/978-1-4614-7324-4_22,

The syntax for specifying these options in the covergroup definition is
option.option_name = expression;

Option Name	Default	Description
weight = *number*	1	If set at the **covergroup** syntactic level, it specifies the weight of this **covergroup** instance for computing the overall instance coverage of the simulation. If set at the **coverpoint** (or **cross**) syntactic level, it specifies the weight of a **coverpoint** (or **cross**) for computing the instance coverage of the enclosing **covergroup**.
goal = *number*	90	Specifies the target goal for a **covergroup** instance, or a **coverpoint** or a cross of an instance.
name = *string*	unique name	Specify a name of the **covergroup** instance. If unspecified, a unique name for each instance is automatically generated by the tool.
comment = *string*	" "	A comment that appears with the instance of a **covergroup**, or a **coverpoint** or **cross** of the **covergroup** instance. The comment is saved in the coverage database and included in the coverage report.
at_least = *number*	1	Minimum number of hits for each bin. A bin with a hit count that is less than *number* is not considered covered.
detect_overlap = *boolean*	0	When true, a warning is issued if there is an overlap between the range list (or transition list) of two bins of a **coverpoint**
auto_bin_max = *number*	64	Maximum number of automatically created bins when no bins are explicitly defined for a **coverpoint**
cross_auto_bin_max = *number*	unbounded	Maximum number of automatically created cross product bins for a **cross**.
cross_num_print_missing = *number*	0	Number of missing (not covered) cross product bins that must be saved to the coverage database and printed in the coverage report.
per_instance = *boolean*	0	Each instance contributes to the overall coverage information for the **covergroup** type. When true, coverage information for this **covergroup** instance is tracked as well.

LRM: SystemVerilog 3.1a, Table 20-1

Fig. 22.1 Coverage options—Reference Material

22.1 Coverage Options: Instance Specific—Example (Figs. 22.1 and 22.2)

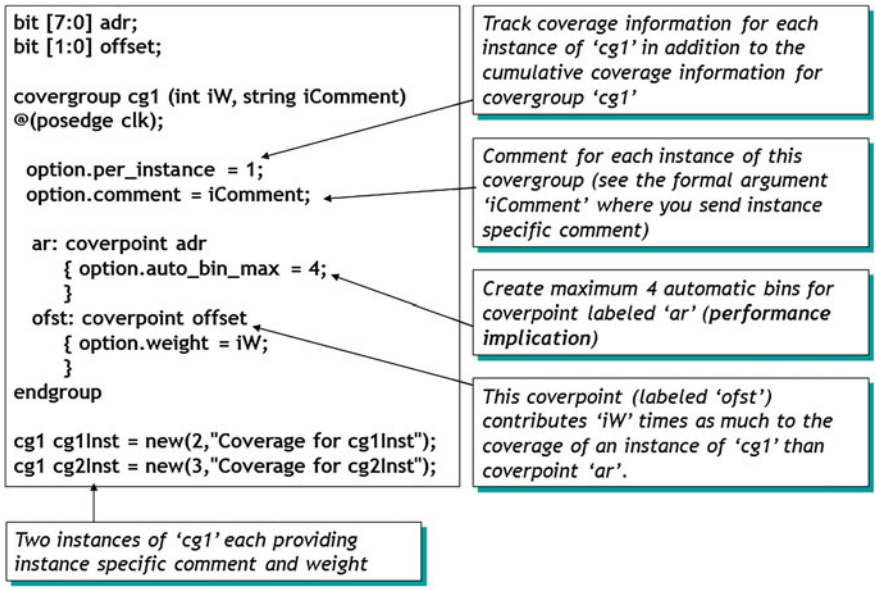


Fig. 22.2 Coverage options—instance specific—Example

22.2 Coverage Options: Instance Specific Per-Syntactic Level (Figs. 22.3 and 22.4)

*The following table summarizes the syntactical level (**covergroup**, **coverpoint**, or **cross**) at which instance options can be specified. All instance options can be specified at the covergroup level. Except for the **weight**, **goal**, **comment**, and **per_instance** options, all other options set at the covergroup syntactic level act as a default value for the corresponding option of all coverpoints and crosses in the covergroup. Individual coverpoint or crosses can overwrite these default values. When set at the covergroup level, the **weight**, **goal**, **comment**, and **per_instance** options do not act as default values to the lower syntactic levels.*

Option Name	Allowed in Syntactic Level		
	covergroup	coverpoint	cross
name	Yes	No	No
weight	Yes	Yes	Yes
goal	Yes	Yes	Yes
comment	Yes	Yes	Yes
at_least	Yes (default for coverpoints & crosses)	Yes	Yes
detect_overlap	Yes (default for coverpoints)	Yes	No
auto_bin_max	Yes (default for coverpoints)	Yes	No
cross_auto_bin_max	Yes (default for crosses)	No	Yes
cross_num_print_missing	Yes (default for crosses)	No	Yes
per_instance	Yes	No	No

LRM: SystemVerilog 3.1a, Table 20-2

Fig. 22.3 Coverage options—instance specific per-syntactic level

The following table lists options that ***describe a feature of the 'covergroup' type as a whole.***
type_option.option_name = expression;

Option Name	Default	Description
weight = *constant_number*	1	If set at the **covergroup** syntactic level, it specifies the weight of this **covergroup** for computing the overall cumulative (or type) coverage of the saved database. If set at the **coverpoint** (or **cross**) syntactic level, it specifies the weight of a **coverpoint** (or **cross**) for computing the cumulative (or type) coverage of the enclosing covergroup.
goal = *constant_number*	90	Specifies the target goal for a **covergroup** type, or a **coverpoint** or **cross** of a **covergroup** type.
comment = *string_literal*	" "	A comment that appears with the **covergroup** type, or a **coverpoint** or **cross** of the **covergroup** type. The comment is saved in the coverage database and included in the coverage report
strobe = *constant_number*	0	If set to 1, all samples happen at the end of the time slot, like the $strobe system task.

LRM: SystemVerilog 3.1a, Table 20-3

Coverage type-options per Syntactic Level

LRM: SystemVerilog 3.1a, Table 20-4

Option Name	Allowed Syntactic Level		
	covergroup	coverpoint	cross
weight	Yes	Yes	Yes
goal	Yes	Yes	Yes
comment	Yes	Yes	Yes
strobe	Yes	No	No

Fig. 22.4 Coverage options type specific per syntactic level

22.3 Coverage Options for 'Covergroup' Type: Example (Figs. 22.5 and 22.6)

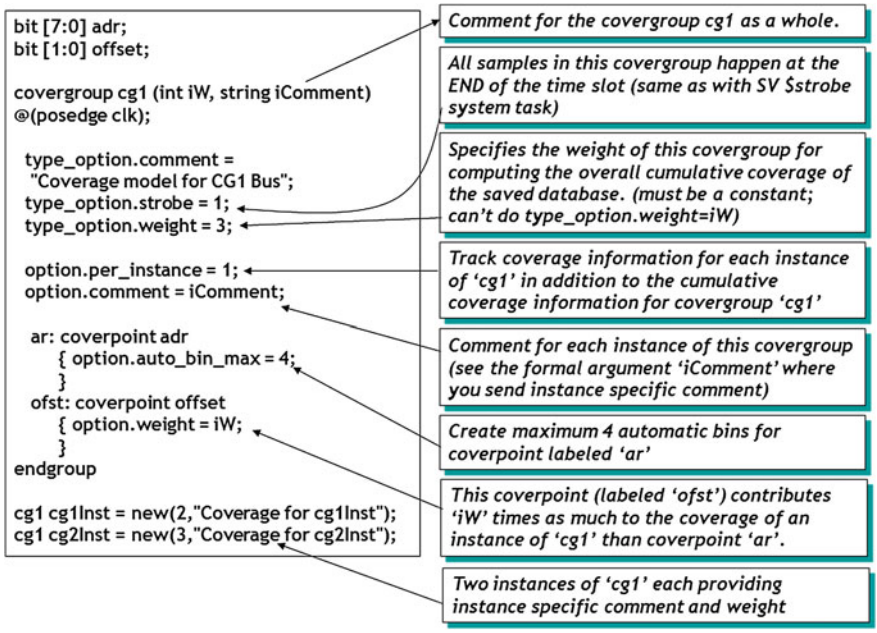


Fig. 22.5 Coverage options for 'covergroup' type specific—comprehensive example

Predefined coverage system tasks and functions	
$set_coverage_db_name (<name>);	Sets the filename of the coverage database into which coverage info. is saved at the *end* of a simulation run
$load_coverage_db (<name>);	Load from a given filename the cumulative coverage information for all the coverage group types.
$get_coverage ();	Returns a real number in the range of 0 to 100 the overall coverage of ***all*** covergroups.

Pre-defined coverage methods used in procedural code

LRM: SystemVerilog 3.1a, Table 20-5

Method	Can be called on			Description
	covergroup	coverpoint	cross	
void sample()	Yes	No	No	Triggers sampling of the covergroup
real get_coverage()	Yes	Yes	Yes	Calculates type coverage number (0...100)
real get_inst_coverage()	Yes	Yes	Yes	Calculates coverage number (0...100)
void set_inst_name (string)	Yes	No	No	Sets the instance name to the given string
void start()	Yes	Yes	Yes	Starts collecting coverage information
void stop()	Yes	Yes	Yes	Stops collecting coverage information
real query()	Yes	Yes	Yes	Returns the cumulative coverage information (for the coverage group type as a whole)
real inst_query()	Yes	Yes	Yes	Returns the per-instance coverage information for this instance.

Fig. 22.6 Predefined coverage system tasks and functions

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DOI: 10.1007/978-1-4614-7324-4,